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Microwave and Millimeter-Wave Signal Power Generation

Dzenan Hadziabdic

March 2009

Abstract

Among the major limitations in high-speed communications and high-resolution radars is the lack of efficient and powerful signal sources with low distortion. Microwave and millimeter-wave (mm-wave) signal power is needed for signal transmission. Progress in signal generation stems largely from the application of novel materials like gallium-nitride (GaN) and silicon-carbide (SiC) and fabrication of indium-phosphide (InP) based transistors.

One goal of this thesis is to assess GaN HEMT technology with respect to linear efficient signal power generation. While most reports on GaN HEMT high-power devices concentrate on one-tone performance, this study also encompasses two-tone intermodulation distortion measurements. An $8GHz$ two-stage power amplifier (PA) MMIC was developed. Harmonic tuning was performed to enhance the power-added efficiency (PAE). The transistors were biased in deep class-AB where low distortion and high PAE were observed. The estimated output power of 42.5 dBm and PAE of at least 31.3% are comparable to the state-of-the-art results reported for GaN HEMT MMIC amplifiers.

Wireless communication systems planned in the near future will operate at E-band, around 71-86 GHz, and require mm-wave-PAs to boost the transmitted signal over distances of 1-2 km. The second goal of this thesis is a technology study and development of an InP HBT based E-band PA. The InP HBT technology was chosen based on the high power density and voltage operation reported for these devices. Characteristics of a 1.5μm InP HBT and a 0.21μm SiGe HBT were compared by means of their models. For that purpose, the SiGe HBT was accurately characterized using VBIC95 model. The modeling work included developing a de-embedding method and application

of direct parameter extraction. The comparison between the HBTs revealed, among others, that SiGe HBT devices operate at a much higher current density and develop a lower junction temperature than the InP HBT. The InP HBT offers, however, higher breakdown voltage. A two-stage InP HBT PA was developed. Record performance are predicted: an output power of $\sim$150 mW with PAE of 15%. The measured gain was 7.5 dB at 77 GHz and relative bandwidth was 45%. Resistive loadings were used to ensure even and odd-mode stability.

Another need in many direct conversion systems and image reject receivers is to generate signals with quadrature offset. Construction of mm-wave quadrature voltage controlled oscillators (QVCOs) is challenging because of the high sensitivity to the circuit parasitics and lack of transistor gain. Third goal of this thesis is to address these problems. Deleterious effects of interconnects and HBT parasitics on a differential oscillator were characterized. A QVCO comprising two coupled differential InP HBT LC-oscillators was developed. A simple method of predicting parasitic oscillations was proposed. The frequency tuning combines modulation of the coupling strength and modulation of the HBT capacitances. An output power of -14.7 dBm per single-ended output and state-of-the-art frequency and tuning range of 37-47.8 GHz were measured. Simulated phase noise ranged from -85 to -88 dBc/Hz at $1MHz$ offset from the carrier.

Resumé

Blandt de vigtiste begrænsende faktorer i højhastighedskommunikation og højopløsning-radarer er forvrængning og en lav effektivitet i effektsignal-kilderne. Høj effekt er nødvendig for transmission af signaler. Fremgang i genereringen af mikrobølge og millimeterbølge (mm-bølge) signaler stammer primært fra anvendelsen af de nye materialer som gallium-nitrit (GaN) og silicium-karbid (SiC) samt fremstilling af indium-fosfid (InP) transistorer.

Et mål med denne afhandling er at vurdere GaN HEMT teknologien mht. lineær og effektiv signalgenerering. Mens de fleste artikler om GaN HEMT effekttransistorer koncentrerer sig om én-tone performances, vil denne undersøgelse også omfatte målinger af to-tone intermodulation-forvrængning. En $8GHz$ to-trins effekt forstærker (PA) MMIC er blevet udviklet. Harmonisk afstemning var foretaget for at forøge effektiviteten (PAE). Transistorerne blev forspændt i klasse-AB, hvor en lav forvrængning og et højt PAE blev observeret. Den estimerede udgangseffekt på 42.5 dBm og mindst 31.3% PAE er i størrelsesorden med de publicerede state-of-the-art resultater for GaN HEMT MMIC forstærkere.

Trådløse kommunikationssystemer planlagt til den nære fremtid vil operere ved E-bånd, 71-86 GHz, og de mangler mm-bølge PA'er, der muliggør trådløs signaltransmission over afstande på 1-2 km. Det andet mål med denne afhandling er teknologiundersøgelse og udvikling af en E-bånds PA. InP HBT teknologi blev valgt pga. de høje effektætheder og operationsspændinger rapporteret for disse transistorer. Egenskaber af en InP HBT og en SiGe HBT blev sammenlignet ved hjælp af deres transistormodeller. Med dette formål blev en $0.21\mu m$ SiGe HBT nøjagtigt karakteriseret vha. VBIC95 model. Modeller-

ingsarbejdet inkluderede udvikling af en 'de-embedding' metode og anvendelsen af direkte parameterekstraktion. Sammenligning mellem HBT'ene afslørede bl.a. at SiGe HBT'en opererer ved meget højere strømtæthed og udvikler en lavere temperatur end den brugte InP HBT. InP HBT'en har dog en højere overslagsspænding. En totrins InP HBT PA er blevet udviklet. Rekord performance niveauer blev simularet: en udgangseffekt på 150 mW samt PAE på 15%. Den målte forstærkning ved 77 GHz var 7.5 dB og Den relative $3dB$ båndbredde var 45%. Resistive belastninger blev brugt for at sikre 'even-mode' og 'odd-mode' stabiliteten.

I mange systemer for direkte konvertering og i modtagere med spejlfrekvensundertrykkelsen er det desuden nødvendigt at kunne generere signaler med kvadraturforhold. Konstruktion af mm-bølge spændingskontrolerede kvadratur-oscillatorer (QVCO'er) er besværlig pga. en høj følsomhed overfor de parasitiske effekter og manglende transistorforstærkning. Det tredje mål med denne afhandling er behandling af disse problemer. Den skadelige indvirkning af forbindelseslinier og HBT'ens parasitiske elementer på en differential oscillator var analyseret. En QVCO bestående af to koblede InP HBT LC-oscillatorer blev udviklet. En simpel metode til at forudsige parasitiske oscillationer er forelagt. Frekvensafstemningen kombinerer modulering af koblingsstyrken og modulering af HBT kapacitanserne. En udgangseffekt på -14.7 dBm per kanalen, samt en state-of-the-art frekvens og afstemningsområde, 37-47.8 GHz, var målt. Den simulerede fasestøj ligger imellem -85 og -88 dBc/Hz ved $1MHz$ afstand fra bærebølgen.

Preface

This thesis was submitted as a part of the requirements to achieve the Ph.D. degree at the DTU Electrical Engineering, Technical University of Denmark. The Ph.D. study was performed from October 1^{st} 2005 to December 31^{th} 2008 and was financially supported by Technical University of Denmark. Professor Viktor Krozer was supervisor for the project together with co-supervisor Associate Professor Jens Vidkjær. Part of the work concerning the development of the GaN HEMT power amplifier has been carried out during the three and half month external research stay at Ferdinand Bran Institute für Höchstfrequenztechnik (FBH), Berlin, Germany.

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Firstly, I would like to thank Professor Viktor Krozer and Associated Professor Jens Vidkjær for their supervision of the project, guidance and support. I appreciate their expertise in their respective fields. I also wish to acknowledge all the Microwave group at DTU Electrical Engineering, and special thanks goes to Professor Tom Keinicke Johansen for providing good transistor models, for fruitful discussions and proofreading the manuscript. I would also like to thank Dr. Torsten Djurhuus and Chenhui Jiang for being helpful during the work. Mogens Pallisgaard is acknowledged for his aid with probestation measurements. Thanks also to Allan Jørgensen from Centre for Physical Electronics (DTU) for quickly resolving any Cadence problem.

In connection with my external stay at FBH, I would like to express my gratitude to Prof. Dr. Wolfgang Heinrich for letting me join his group. I am indebted to Dr. Matthias Rudolph for excellent supervision of my work at FBH. I also sincerely thank all the people from the Microwaves group and the GaN Electronics group at FBH for being so friendly and helpful during my stay in Berlin.

My final thanks goes to Alcatel-Thales III-V Lab for fabricating power amplifier and QVCO chips. I greatly acknowledge Dr. Agnieszka Konczykowska for immediate support during the circuit developments.

Kgs. Lyngby, March 2009

Dzenan Hadziabdic

Publication List

As a part of the dissertation work, the following publications have been prepared:

1. D. Hadziabdic, T. Johansen, V. Krozer, A. Konczykowska, M. Riet, F. Jorge, and J. Godin, "47.8 ghz inp hbt quadrature vco with 22% tuning range," *Electronics Letters*, vol. 43, no. 3, pp. 153-154, 2007.

2. D. Hadziabdic, C. Jiang, T. Johansen, G. Fischer, B. Heinemann, and V. Krozer, "De-embedding and modelling of pnp sige hbts," *EuMIC 2007, European Microwave Integrated Circuits Conference*, pp. 195-198, 2007.

3. D. Hadziabdic, V. Krozer, and T. K. Johansen, "Power amplifier design for e-band wireless system communications," *EuMC 2008, Proceedings of the 38th European Microwave Conference*, pp. 1378-1381, 2008.

4. D. Hadziabdic and V. Krozer, "Power amplifier technology at microwave and millimeter-wave frequencies: an overview," *GeMiC 2008, German Microwave Conference*, 2008.

5. T. K. Johansen, V. Krozer, J. Vidkjaer, D. Hadziabdic, and T. Djurhuus, "Millimeter-wave integrated circuit design for wireless and radar applications," *24th Norchip Conference*, pp. 257-260, 2007.

Contents

Chapter 1

Introduction

This chapter will first introduce the general background and research focus of this work. Thereafter, a thesis overview will provide more detailed explanation of the problems to be dealt with in the thesis.

1.1 Background and Research Focus

Systems for communications and radar applications operating at microwave (1-30 GHz) and millimeter-wave (30-300 GHz) frequencies require efficient generation of signal power. The efficient signal power generation is an area of importance for industry, and research is ongoing in application areas such as base stations for mobile communications, wireless broadband and radar systems. Signal power is needed for signal transmission and its generation is limited by the device performance. Distortion in communication channels and radar applications originates to a large extent from power amplifiers (PAs). Moreover, power consumption in a transmitter is highly dependent on power amplifier's efficiency. This thesis attempts to find best combination of technology and circuit to obtain optimum performance.

Many satellite transmitters and base stations for microwave communications still use vacuum tubes in the power amplifiers, especially when high power levels, such as hundreds or thousands of Watts, are needed. Improvements in solid-state technology developments enable replacement of the vacuum tubes with semiconductor devices that

are lighter and have longer lifetime. Gallium-nitride (GaN) is a wide-bandgap material projected to overcome the current power limitations of silicon (Si) and gallium-arsenide (GaAs) based devices. GaN based high electron mobility transistors (HEMTs) supporting high voltages and currents have been reported by many groups [1–4]. Some of the interesting applications are cellular phone base-stations, fixed point-to-point microwave links, satellite communication systems and radar applications ranging up to Ka-band (26.5-40 GHz).

One objective of this thesis is to investigate the possibilities of the GaN HEMT technology for linear and efficient signal power generation. Reported results on GaN-based high-power devices and amplifiers mainly concentrate on one-tone output power and efficiency performance. The signal generation in this thesis will rely on one-tone and two-tone experiments and a design of an $8GHz$ monolithic microwave integrated circuit (MMIC) PA addressing high power, linearity and efficiency. The $8GHz$ power amplifier has potential application in X-band satellite uplink communication systems. X-band frequency range has been historically reserved to support the government and military communication needs in number of countries. Various communication satellites including WGS, XTAR-EUR, DCSC, Spainsat, Koreasat and Skynet, uses the 7.25-7.75GHz range for downlink and 7.9-8.4GHz for uplink data transmission.

Among the promising application fields for millimeter-wave power amplifiers are 76-77 GHz automotive radars, W-band (75-105GHz) military radars as well as the two emerging high-capacity wireless communication systems operating in 57-64GHz range and at E-band, respectively. Wide bandwidths available for these two communication standards enable data transmission beyond 1 Gb/second. Such data rates exceed the possibilities of nowadays microwave communication links, as indicated in Fig.1.1.

High attenuation in the atmosphere around 60 GHz, 10-15 dB/km, mainly caused by oxygen molecular absorption [6, 7], makes this frequency range suitable for all kind of short-range wireless communications such as wireless local/personal area network (WLAN/ WPAN) applications [8, 9].

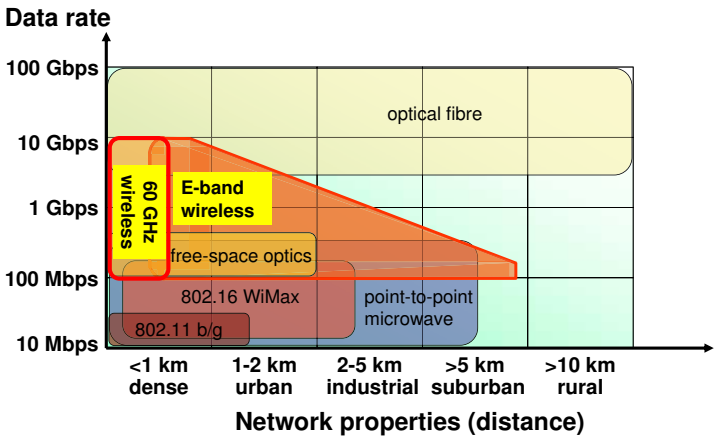

Figure 1.1: Data capacities plotted versus distances for various microwave and mm-wave communication systems indicate market potential of E-band systems [5].

The E-band refers to a 10 GHz licensed spectrum split into two bands, 71-76 GHz and 81-86 GHz, respectively. It is suitable for long-range data transmission between two fixed locations, since the two bands occur within the 'atmospheric window', where the attenuation is relatively low, 0.2-1 dB/km. The attenuation, however, substantially increases with rate of rainfall [7]. The full allocated 71-76GHz spectrum may be used for transmission from one side, and the 81-86 GHz spectrum from the other side of a full-duplex communication link [10]. Requirement to concentrate the emitted power in a narrow beam allows large number of point-to-point links within a small geographic area.

E-band wireless communications will become important as the microwave backhaul for high-speed data transmission. Increasing demands for high data-rates necessitate use of spectrally efficient modulation schemes, which in turn require linear power amplification. A solution is to operate the amplifier at lower power levels (in back-off). As the generation of E-band signal power is already difficult enough owing to device scaling, the high-power amplifiers are considered to be one of the most critical components of E-band communication systems. An E-band power amplifier is typically required to deliver an

output power of P_{out}>$100mW$. In this thesis, design of E-band PA MMIC complying with this requirement was undertaken. The design was based on InP heterojunction bipolar transistor (HBT) technology.

The choice of InP HBT technology relied on a detailed analysis of the capabilities of commonly utilized MMIC technologies. Nowadays mm-wave power MMICs based on silicon-germanium (SiGe) HBT technologies have similar power and efficiency performance to those of the InP HBT MMICs, despite of quite different material properties. A deeper understanding of the characteristics of the two HBT technologies will be obtained by comparing the model parameters and simulated performance of two specific HBTs. For that purpose, a large-signal modeling of a mm-wave SiGe HBT will be demonstrated in this thesis. Modeling of the InP HBT has been performed elsewhere [11].

Besides power amplifiers, communication systems require low-phase-noise tuneable oscillators. Millimeter-wave oscillators are required to generate ever increasing frequencies, and generation of an adequate signal power becomes difficult. Moreover, signals with quadrature phase relationship are of particular importance for quadrature (de)modulators, direct-conversion transceivers and image rejection mixers. Only limited work has been published on design and analysis of mm-wave quadrature voltage controlled oscillators (QVCO). Construction of mm-wave QVCOs is challenging, because the performance is limited by circuit complexity, lack of transistor gain and high conductor losses. These problems are addressed in this thesis through the design of a monolithic mm-wave QVCO. High oscillation frequency is the main goal of this work. This will also become a first QVCO developed in InP HBT technology.

1.2 Thesis overview

The main part of the thesis is divided into eight chapters.

Chapter 1 began with an introduction to this work.

Chapter 2 continues the introductory part. The developed PA and QVCO MMICs are discussed as building blocks of two generic communication transmitters: an X-band phased array for mobile satellite uplink, and an E-band transmitter for fixed point-to-point link.

Chapter 3 puts the GaN HEMT technology into perspective with other solid-state technologies considering efficient high-power generation at X-band. The chapter will thereafter review state-of-the-art with regards to different technologies employed in the manufacturing of mm-wave power amplifiers and oscillators. The motivation for the choice of the InP HBT technology for E-band power amplifier and QVCO will be explained. Basic description of the investigated processes will be given. These are: $0.35\mu m$ GaN HEMT, $1.5\mu m$ InP HBT and BiCMOS process containing $0.21\mu m$ SiGe HBT. Accuracy of available transistor models will also be discussed.

Chapter 4 presents the development of GaN HEMT amplifier including the two-tone characterization of the device intermodulation distortion, bias point selection and the applied second harmonic manipulation technique for PAE enhancement.

Chapter 5 compares the SiGe and InP HBT model parameters and simulations with respect to E-band signal power generation and amplification. In connection with this, detailed description of a small-signal and VBIC95 model parameter extraction for SiGe HBT is given together with a suggested technique for de-embedding of the test-structure parasitics. Preliminary considerations regarding the InP HBT E-band power amplifier design are outlined.

Chapter 6 continues with the E-band PA development. Common mm-wave amplifier configurations will be investigated with respect to electrical stability and gain performance. Details of the design approach, methods applied for even and odd-mode stability analysis and achieved performance will be presented.

Chapter 7 is dedicated to the development and characterization of a QVCO. The open-loop analysis explores the effects of various passive and HBT parasitics on oscillation frequency and quality factor in two different mm-wave oscillator topologies. Design guidelines to suppress these degradations are suggested. Frequency tuning mechanisms and their mutual interactions are discussed. A potential instability within the QVCO is identified and measure to prevent this instability is presented.

Chapter 8, finally, summarizes the conclusions of this thesis.

Chapter 2

Signal Generation in Transmitter Front-Ends

Transmitters and receivers in microwave and millimeter-wave wireless communication links encompass digital and analog subsystems and antennas. In this chapter, the MMICs developed in this thesis will be viewed as building blocks in communication transmitter front-ends.

One promising application for the linear efficient GaN HEMT X-band power amplifier MMIC is phased array for mobile satellite communications. Basic description of the phased array transmitter will be provided with emphasis on the beam forming network.

InP HBT MMICs designed in this thesis are power amplifier and QVCO. The suggested transmitter for E-band communications will serve as the potential application example for the two MMICs. The upconverter subsystem employs a sub-harmonic mixer to enable use of the QVCO operating at around half of the desired frequency.

2.1 X-band Phased Array

Phased arrays for satellite communications have been developed for both submarine, naval, airborne and terrestrial use [12–14]. They are widely used for these purposes because they allow electronic beam-forming, resulting in more reliable operation in comparison to mechanically steered antennas.

Fig.2.1 shows the basic architecture of the phased-array involving a frequency upconverter, beam-forming network (BFN) and antennas arranged into one-dimensional array. The BFN consists of driver amplifier (DA), power dividers, variable phase-shifters and output power amplifier (PA) MMICs. The elevation of the antenna beam is electronically controlled by adjusting the relative phase-shift of the feeding signals. The phased arrays are often two-dimensional, which makes it possible to steer the beam in azimuth direction as well. Here mechanical control is assumed in azimuth. The upconverter is needed to translate the modulated signal at intermediate frequency (IF) to RF frequency which is between 7.9 and 8.4 GHz for the X-band uplink applications. The RF signal is then amplified by the driver amplifier DA to obtain sufficient power level. The power signal is equally split into eight channels using the Wilkinson power dividers. The objective of this work is to develop the PA MMIC building block.

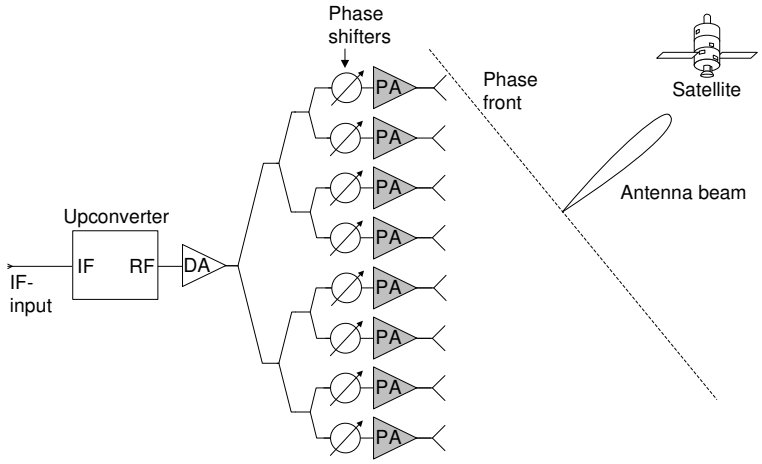

Figure 2.1: Basic configuration of the X-band phased array.

At high power levels, where voltage and current excursions in a transistor reach their limits, output signal becomes distorted. An undesirable consequence of the signal distortion in X-band satellite communications is adjacent channel interference [15]. Moreover, the power amplifier distortion can increase symbol-error probability in communication links [16]. A simple way to study the nonlinear transistor behav-

ior is to measure the third order intermodulation distortion (IMD3), when the transistor is excited by two tones at frequencies f_A and f_B, respectively. Then the expression for IMD3 is

$$IMD3 = \frac{P_o}{P_{IM3}} \tag{2.1}$$

where P_o is the output power at one of the fundamental tones (at f_A or f_B) and P_{IM3} is the output power of one of the intermodulation products (at $2f_A - f_B$ or $2f_B - f_A$). Such test has been carried out during the power amplifier design and will be described in chapter 4.

Forcing the transistors into gain compression is not desirable with respect to the signal distortion. Transistors, however, tend to operate most efficiently under this regime. Power added efficiency (PAE) is a conventional measure of an amplifiers ability to convert DC-power and input signal power into the useful output signal power. The PAE is given by

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \left(1 - \frac{1}{G_P}\right) \tag{2.2}$$

where P_{out} is the output power, P_{in} is the available input power, P_{DC} is the consumed DC-power and G_p is the available power gain of the amplifier. According to the eq.(2.2), the PAE tends to increase with P_{out}. In practice, however, the PAE starts to drop above certain input power level at which G_p is sufficiently compressed. Low P_{DC} at high P_{out} results in high PAE and reduced device junction temperature with a consequent improvement in reliability. Moreover, the amplifiers PAE is of vital importance for battery lifetime and heat generation in portable and spaceborne applications.

Power gain is another important parameter of the PA MMIC in the phased-array example in the Fig.2.1. Suppose that the PA MMIC also can serve as the DA driver amplifier. If the DA MMIC should be able to drive eight PAs, the PAs must provide sufficient gain. In order to estimate the minimum required gain, it will be assumed that the phase-shifter and Wilkinson divider exhibit $4dB$ and $0.5dB$ loss as reported in references [17] and [18], respectively. The required drive level becomes

$$P_{DA} = P_{PA} - G_{PA} + 4 + 10\log_{10}(8) + 3 \times 0.5 \quad [dB] \tag{2.3}$$
$$= P_{PA} - G_{PA} + 14.5 \quad [dB] \tag{2.4}$$

where G_{PA} is the power gain of the PA, P_{PA} and P_{DA} are the output powers of the PA and DA MMICs, respectively. If the PA MMIC also should be useful as the DA driver, this would imply P_{PA}=P_{DA} in the equation above. Hence, the minimum required gain would become G_{PA}=14.5 dB. Obviously, larger G_{PA} would relax the requirement on the DA output power capability. The gain requirement of >14.5 dB calls for two-stage solution, since X-band MMIC power amplifiers usually exhibits around 8-12 dB gain per stage [19–36].

2.2 E-band Transmitter

Quadrature oscillators are often used in quadrature (de)modulators, direct-conversion systems and subharmonic mixers. Design of quadrature oscillator operating at E-band spectrum 71-86 GHz is highly challenging, because of the lack of transistor gain, high conductor losses and circuit complexity, all of which limit the generated signal power. One solution to this problem is to employ a sub-harmonic mixer, which uses a double of the oscillator frequency. Basic transmitter structure incorporating such a mixer is depicted in the Fig.2.2. The power amplifier (PA) and local oscillator (LO) for this system were developed during this thesis. Various active double-balanced subharmonic mixers requiring quadrature LO signals have been reported in references [37–39].

The incoming signal V_{IF} is modulated using an intermediate frequency f_{IF}. The IF frequency is assumed to be 2.5 GHz. The IF-spectrum is then upconverted by the mixer to the E-band frequency range. The mixer is pumped by the two LO signals amplified by the two buffers. The two LO signals at frequency f_{LO} are 90° out of phase. The upper sideband RF frequency is then

$$f_{RF} = 2f_{LO} + f_{IF}. \tag{2.5}$$

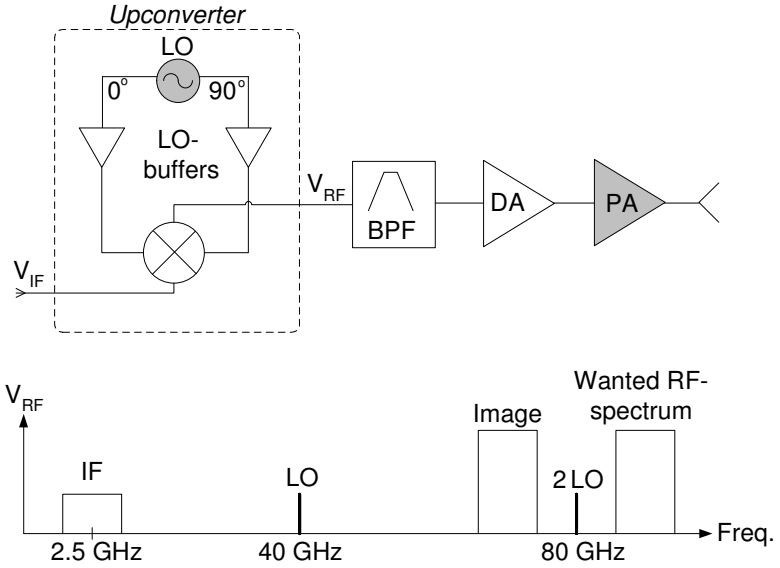

Figure 2.2: E-band transmitter front-end. Up: basic transmitter architecture. Down: frequency spectrum at the output of the upconverter.

The second harmonic of the local oscillator, $2f_{LO}$, which falls near the desired RF band, tend to be suppressed in sub-harmonic mixer [37,40]. The undesired components like LO-leakage at f_{LO}, IF-leakage at f_{IF} and image frequency $2f_{LO}$-f_{IF} are removed by the band-pass filter (BPF).

In fundamental mixers where LO frequency is near the RF frequency, high-power RF signal at the PA output can couple to the LO, which perturbs the LO, causing undesired spurs in the oscillator spectrum [41]. Sub-harmonic mixers, however, do not suffer from this drawback, since LO oscillates far away from the RF signal frequency [42,43].

Anyway, every oscillator exhibits fluctuations of the generated frequency in time - a phenomenon known as phase noise [44]. Oscillator phase noise originates from the noise sources of the devices in the oscillator itself as well as from the externally injected noise. The actual frequency spectrum of the LO is not an ideal impulse function, but rather a continuous spectrum with non-zero bandwidth centered on

f_{LO}. Hence, the mixer is not driven by an ideally stable frequency. As a result, the information carried in the phase of the RF carrier is corrupted, leading to increased bit-error rate in a communication link [41]. An analytic expression for phase-noise will be presented in next chapter in connection with technological considerations.

The design goals for the mm-wave MMICs:

Typical specification for an E-band power amplifier is $P_{out} > 100$ mW (20 dBm). The two bands of interest are 71-76GHz and 81-86GHz. In chapter 5 it will be shown that the available power gain of the used InP HBT transistors was 6.3 dB in the lower band. In the upper band the power gain was only 5.15 dB which was considered to be suboptimal gain for the design of a power amplifier MMIC in that range. The amplifier was therefore developed targeting the lower E-band, 71-76 GHz.

On the other hand, oscillation frequency of a quadrature oscillator is not only dependent on the transistors, but also on size of passive elements and interconnect parasitics. Main motivation behind the QVCO design was a high oscillation frequency. The LO frequency of 40GHz, used in the shown E-band transmitter, turned out to lie within the obtained tuning range. As such, the designed QVCO could be utilized to cover the upper E-band, 81-86 GHz when integrated in the discussed transmitter from Fig.2.2.

Chapter 3

MMIC Technologies for Signal Generation

A variety of solid-state technologies for manufacturing of MMICs exists today. Transistors play a key role in power amplifier and oscillator performance. Transistor characteristics strongly depend on properties of the semiconductor materials. This chapter will start with brief comparison of the fundamental properties of common semiconductor materials including silicon, gallium-arsenide, indium-phosphide, gallium-nitride and silicon-carbide. This discussion will form a basis for the subsequent comparison of modern solid-state technologies.

GaAs based HEMTs and HBTs have established a strong position in the efficient power generation at X-band. In recent years, however, GaN HEMT technology has emerged as a promising candidate for microwave high-power applications. GaN HEMT technology will be used for the X-band high-power amplifier design. The motivation for using the GaN HEMT technology is based on the reported high-power and high power-density results.

For the power generation at E-band frequency range around 70-90 GHz there are only few solutions available today, most of these involving HEMT device technologies. However, InP HBT devices offer a good alternative for power amplification due to the very high power densities and breakdown voltages. These properties have motivated selection of InP HBT technology for the E-band amplifier design.

Only limited work has been published on mm-wave QVCOs. Main attention have been paid to silicon type solutions primarily due to possibility for integration with other analog and digital circuits [45–49]. Before this work no InP HBT based quadrature VCOs have been published. High gain and low 1/f noise of the InP HBT transistors as well as low-loss InP substrate have motivated the investigation of InP HBT technology for the QVCO design.

Last part of this chapter provides basic description of the actual $0.35\mu m$ GaN HEMT and $1.5\mu m$ InP HBT processes selected for the designs. An additional BiCMOS process containing $0.21\mu m$ SiGe HBT will also be described. Later in chapter 5, capability of the SiGe and the InP HBTs to serve as E-band amplifiers will be discussed.

Accuracy of the available transistor models will also be investigated. An experimental characterization of the GaN HEMT power device will be described, in order to provide verification of the provided transistor model. It will be shown that the model was not accurate at higher drive levels.

InP HBT models were proven to be reasonably accurate when compared to the DC and small-signal measurements.

Model development of the SiGe HBT will be treated in chapter 5.

3.1 Semiconductor Materials

The Johnson figure of merit [50] has been defined to assess the power and frequency performance limits of transistors. The figure of merit is defined as

$$f_t\sqrt{P_{max}X} = \frac{E_{max}v_s}{2\pi} \tag{3.1}$$

where f_t is the cut-off frequency, defined as a frequency where the current gain drops to unity, P_{max} is the maximum output power, X is the reactance of the collector-base (drain-gate) capacitance at f_t, and v_s and E_{max} are, respectively, maximum carrier velocity and breakdown field. The right-hand side of the equation is determined by the semiconductor material properties and the left-hand side by device parameters. This figure of merit sets the limits for the maximum power that can be delivered by the device having given impedance and f_t.

Table 3.1 compares the basic material properties of various semiconductors. Thanks to the relatively high bandgap energy, the breakdown field E_{max} of a GaN material is more than six times that of InP, GaAs and Si. This permits high supply voltage to be applied, which in turn enables high voltage swing and output power.

High power generation also requires a semiconductor that supports high current. Maximum density of current flow through a material depends on the maximum electron velocity. An outstanding combination of high bandgap and electron velocity makes the GaN material most suitable for high-power transistors, according to the Johnson limit.

For the devices operating at high voltages and high currents, good thermal conductivity of the semiconductor substrate material is essential, because it indicates its ability to remove the heat generated by the device. GaN based transistors are mostly grown on silicon-carbide (SiC), which offers superior thermal conductivity among the common semiconductor materials, according to the Table 3.1.

	Si (—)	GaAs (AlGaAs/ InGaAs)	InP (InAlAs/ InGaAs)	SiC (—)	GaN (AlGaN/ GaN)
Bandgap $[eV]$	1.1	1.42	1.35	3.26	3.49
Breakdown field $[MV/cm]$	0.3	0.4	0.5	2.0	3.3
Electron mobility $[cm^2/V\text{-}s]$	1500	8500 (10000)	5400 (10000)	700	900 (>2000)
Saturated/peak electron velocity $[\times 10^7 cm/s]$	1.0/ 1.0	1.0/ 2.1	1.0/ 2.3	2.0/ 2.0	1.5 / 2.7
Thermal conductivity $[W/cm\text{-}K]$	1.5	0.5	0.7	4.5	>1.7

Table 3.1: Basic properties of commonly utilized semiconductor materials.

Most investigation on GaN devices has focused on AlGaN/GaN HEMTs. This work has been largely limited to the last decade, and in spite of the rapid progress, nowadays GaN HEMT processes are still relatively immature in comparison to those based on the conventional

materials such as Si and GaAs. Due to this fact, power GaN HEMTs are still mainly utilized at frequencies ranging up to 40 GHz. Recent developments, however, demonstrated that the GaN device technology has a good prospect for power applications even at 80 GHz [51].

Transistors based on Si and GaAs have found applications in much broader frequency range. Silicon based devices such as SiGe HBT benefits from a good thermal conductivity of that material. However, low dielectric breakdown field and peak velocity pose significant power and speed limitation. Despite of this fundamental disadvantage, power amplifier MMICs targeting automotive radar applications at $77GHz$ have been demonstrated [52]. High-frequency gain improvements arise in part from the downscaling of the device junctions and parasitics.

AlGaAs/GaAs based HBTs deliver remarkably higher microwave power than SiGe HBTs because of the larger bandgap, superior electron mobility, and higher peak velocity of the GaAs material. GaAs based pseudomorphic HEMTs (pHEMTs) utilizing AlGaAs/InGaAs heterostructures have found almost universal application at microwave and mm-wave ranges up to about 100 GHz. High-power performance of GaAs transistors is mainly limited by the inferior thermal conductivity of that material.

InP baseline material provides several advantages compared to GaAs: higher thermal conductivity, higher breakdown field and higher peak velocity. InP HBTs have the highest frequency performance among bipolar transistors. The InP/InGaAs heterostructure emitter allows ballistic injection of electrons into the InGaAs base [53]. Resultant average velocity of the electrons traversing the thin base and collector space-charge region can be higher than 5×10^7 cm/s [53], which is a twofold increase with respect to the maximum steady-state velocity. This enhances high-frequency performance by reducing the overall transit time and corresponding base emitter diffusion capacitance. The velocity overshoot effects also occur in GaAs HBTs, though at lower extent, as well as in III-V based field effect-transistors [53].

3.2 Technology Comparison

3.2.1 X-band High-Power MMICs

In Fig.3.1 (left plot) the reported PAE of the state-of-the-art MMIC power amplifiers operating at X-band frequency range of interest is depicted versus their saturated output power. The shown PAE refers to the peak value, which is usually reached at higher power levels, where the amplifier gain is compressed by 1-3dB below the small-signal value. In Fig.3.1 (right plot) the PAE is plotted versus total gate width of the amplifier's output stage. It can be inferred from the plots that the GaN HEMT amplifiers are capable of delivering higher powers as compared to GaAs HEMTs despite of their smaller peripheries. This superior power density is in accordance with the abovementioned advantages of the wide-bandgap material. Two circuit related advantages arise from the high power density of GaN HEMT devices. Firstly, larger power per MMIC area can be obtained because smaller semiconductor area is devoted to transistors and on-chip combining circuitry. Secondly, smaller device periphery for a given output power implies larger device impedance, and consequently, an easier matching of very large devices to a 50-Ω environment.

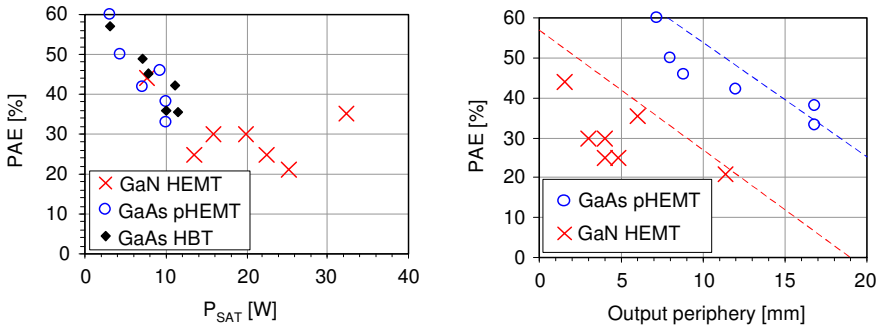

Figure 3.1: Comparison involving GaAs HBT [19–24], GaAs pHEMT [25–30] and GaN HEMT [31–36] PA MMICs with competing performance in 8-10GHz range.

It is finally worth to note the trade-off relationship appearing between the achieved power and PAE in the Fig.3.1 (left plot). This

trade-off is partly a consequence of increased combining losses occurring when power from very large output peripheries is combined on chip. Mutual heating between the adjacent fingers of very large devices and unequal contribution of device fingers to the output power also degrade the efficiency of a high-power amplifiers. Same conclusions follow from the right plot, where PAE versus output periphery follows a similar trend to that in the left plot.

3.2.2 Millimeter-Wave Power MMICs

At X-band frequency range GaAs HBTs compete with GaAs pHEMTs with respect to power and efficiency, as it was depicted in the Fig.3.1. The HBTs are often stated to be attractive devices for high-power applications because of their high power densities arising from vertical current flow through the device area. Above roughly $30GHz$, however, GaAs HBTs are seldom utilized in power MMICs. Their pHEMT counterparts benefit from a superior velocity and mobility of a 2-dimensional electron gas formed in the heterostructure channels, which allows these transistors to achieve high gain well into millimeter wave region.

Unique attributes of the indium-phosphide material system enable fabrication of HBT power MMICs providing adequate gain at frequencies exceeding 100 GHz. As depicted in the Fig.3.2 (left plot), reported InP HBT amplifiers exhibit very high power densities outperforming all HEMT technologies in the entire frequency range. However, at the same time the peripheries of InP HBT based amplifiers are relatively small, as can be depicted in the right plot.

When larger peripheries are considered, HEMT devices clearly outperform HBT type technologies in the delivered power, as depicted in the Fig.3.3. One of the reasons for the small periphery for the InP HBT technology is the focus on optoelectronic high speed circuit rather than analog circuit applications. From the Fig.3.3 it can be concluded that with an output power of around 100 mW and power-added efficiencies of around 15%, InP HBT technology would start being comparable to the HEMT type of technologies. InP HEMT today represents state-of-the-art performance for the frequency range above 60 GHz. It should

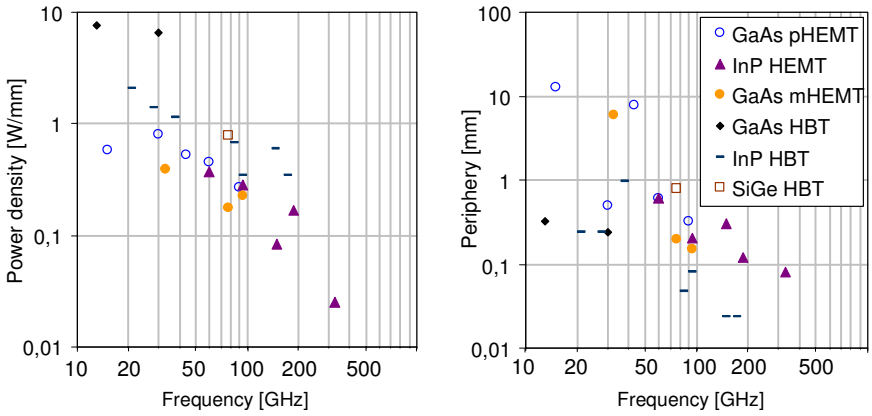

Figure 3.2: Left: Highest power densities reported for GaAs pHEMT [54–58], InP HEMT [59–63], GaAs mHEMT [64–66], GaAs HBT [67, 68], InP HBT [69–75] and SiGE HBT [52] monolithic PAs. Power density is calculated as the delivered power per total emitter length (for HBTs) or gate width (for FETs) in the MMIC output stages. Right: Total output peripheries for the same group of amplifiers.

be noted that InP HEMT amplifier module delivering 1 W V-band power (see Fig.3.3) employs two externally combined channels on a single MMIC. Moreover, the results for SiGe HBT are at lower frequencies compared to most of the results on InP HBT and HEMT technologies.

Beside the InP HBT, the SiGe HBT technology also delivers high power density, as it was shown in the Fig.3.2 (left plot). While InP HBTs benefit from attractive material properties, the SiGe HBTs are more down-scaled both in lateral dimensions and emitter current density [89]. In contrast to high current density, high breakdown voltages and the according bias conditions facilitate PAE and improve the matching design. In principle, the same arguments apply at mm-wave frequencies as those at microwave frequencies with regards to the advantages of GaN technology. Also at mm-wave frequency the technology with a high breakdown voltage will have a fundamental advantage in power amplifier design. The implication of the breakdown voltage can be viewed from the data available on the bias voltage for the respective technology. In Fig.3.4 the available data on the bias

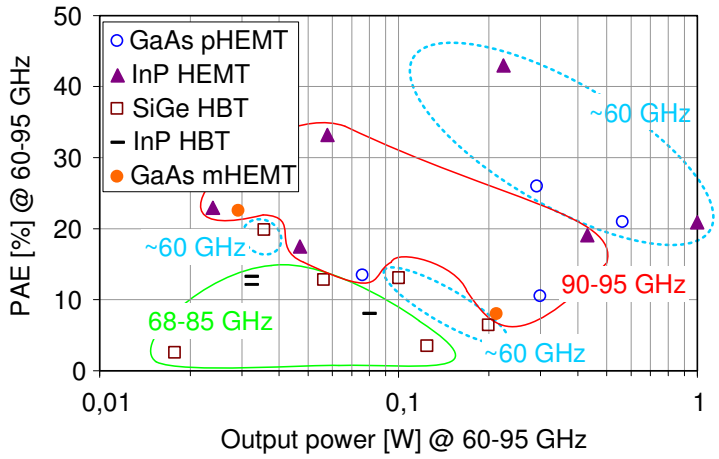

Figure 3.3: Power added efficiency versus output power reported for GaAs pHEMT [54, 76, 77], InP HEMT [59, 61, 78–80], GaAs mHEMT [64, 81], InP HBT [70, 82, 83] and SiGe HBT [52, 84–88] monolithic amplifiers. It is believed that solutions exhibiting record powers and PAE for the particular technologies are included.

voltage are shown versus frequency. It can be depicted that InP HBT technology offers among the highest voltages above $60GHz$ and has an intrinsic advantage when scaling to higher frequencies, as demonstrated by the data beyond 100 GHz.

From the above discussion it is clear that the InP HBT technology is a promising candidate for power amplifier design at E-band frequencies, 71-86GHz.

3.2.3 Oscillator MMICs

As mentioned in connection with the E-band upconverter, phase noise causes the local-oscillator signal to spread in frequency. Leeson [44] derived an equation describing the single-sideband phase noise power density spectrum in a linear model of an oscillator. When the 1/f noise contribution from the transistor is neglected, the Leeson model reads

$$L(f_m) = \frac{FkTf_0^2}{8P_{sig}Q^2f_m^2} \quad [Hz]^{-1} \tag{3.2}$$

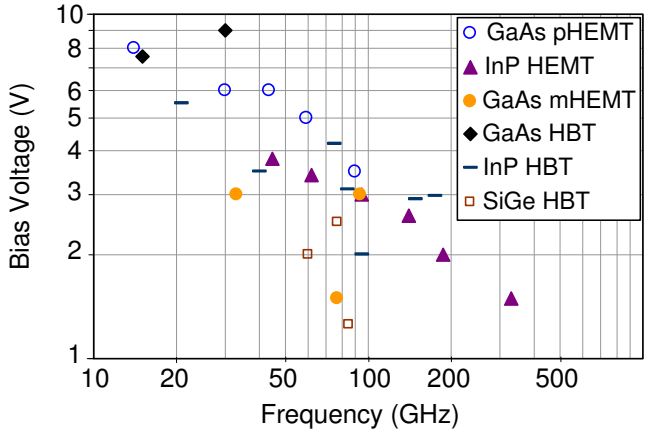

Figure 3.4: Highest bias voltages reported for GaAs pHEMT [54, 58, 90–92], InP HEMT [62, 63, 78, 80, 93, 94], GaAs mHEMT [65, 66, 81], GaAs HBT [68, 95], InP HBT [69–71, 82, 96] and SiGe HBT [84, 86, 88] monolithic amplifiers. The cascode amplifiers share the external bias voltage between common base and common emitter devices. If the voltage across each device was reported, the larger of the two is shown here. Otherwise the reported bias voltage is divided by two.

where, F is effective noise factor that describes a transistor under large signal excitation, k is Boltzmann's constant, T is temperature in Kelvin, P_{sig} is the signal power and Q is the quality factor of a loaded parallel LC-resonator. According to this equation, the phase-noise $L(f_m)$ decreases with the frequency offset f_m from the carrier frequency f_0. The rate of decrease is -20dB per decade, but below certain f_m, the value of which depends on the transistors 1/f noise contribution, this rate increases to -30dB per decade [44].

To date, HEMT technologies have been used to demonstrate mm-wave power amplifiers with record output power levels. On the other hand, the 1/f noise of the HBTs is known to be lower. Hence the HBTs are more attractive for low-phase-noise oscillators as compared to HEMTs. Fig.3.5 compares the published record phase-noise levels for the oscillators implemented in most MMIC technologies. It can be concluded from the figure that the HBT solutions outperform the field-effect-transistor solutions across whole frequency range.

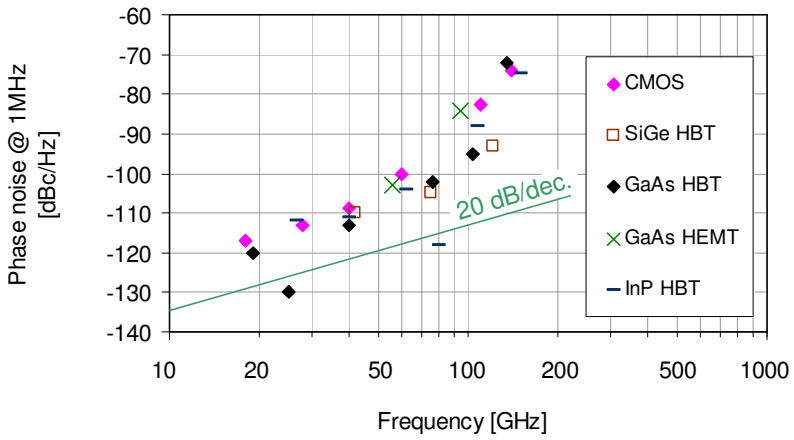

Figure 3.5: State-of-the-art phase noise at $1MHz$ offset reported for fully monolithic oscillators in GaAs HBT [97–101], GaAs HEMT [102, 103], InP HBT [104–108], SiGe HBT [109–111] and CMOS [112–116] technologies.

Quality factor Q is another key parameter controlling the phase noise in a LC-oscillator, as suggested by the eq.(3.2). Hence, low-loss reactive components are desirable for the low-noise LC-oscillator design. Inductors realized on GaAs and InP tend to have higher unloaded Q, as compared to those on Si. This is a direct consequence of the conductive nature of Si as opposed to the insulating nature of the InP and GaAs substrates.

Quality factor of a LC-resonator degrades due to resistive loading by the transistor parasitic resistances. One way to preserve high Q is to reduce coupling between the resonator and the transistor [117–119]. This unfortunately reduces the oscillator loop gain which has to be higher than unity in order to assure oscillation startup. Therefore, the transistor power gain is a relevant parameter for realization of a low-noise high-frequency oscillator. As it follows from the Leeson's equation (3.2), phase noise increases with the oscillation frequency f_0 if the other parameters are kept constant. This rate of increase is represented by the solid line having 20 dB/decade slope in the Fig.3.5. Apparently, the reported oscillators approximately follow this rate of degradation up to 60-70 GHz, but beyond this point, the overall rate

becomes more and more rapid. One likely reason for such trend is that conductor loss increases and hence Q-factor decreases in frequency due to the skin effect, since the current flow becomes confined to the conductor surface, which depth is proportional to $1/\sqrt{f_0}$ [120]. In addition, lack of high-gain transistors at very high frequencies necessitates stronger coupling of the resonators to the transistors, which causes the loaded Q to drop in the very high frequency oscillators.

To date, InP HEMT and InP HBT technologies have been used to demonstrate oscillators operating at highest oscillation frequencies, 346 GHz [121] and 311 GHz [122], respectively. The impressive -118dBc/Hz phase noise at 1MHz offset from 80GHz carrier [105] has been demonstrated in InP HBT technology, as depicted in the Fig.3.5. However, to the author's knowledge, no InP HBT mm-wave quadrature oscillators have been demonstrated yet. Low phase-noise QVCOs are preferably constructed by coupling two identical LC-oscillators. Achievement of a high oscillation frequency is impeded by the design complexity and additional layout parasitics. Hence, the reported QVCOs are largely limited to 40GHz range [45–49].

From the results presented in this section, it is concluded that InP HBT technology is an interesting candidate for the mm-wave QVCO design, and it will be utilized in this work.

3.3 GaN HEMT Technology

The idea behind high electron mobility transistor (HEMT) is to separate the drift electrons from the dopants in order to obtain high mobility. Schematic cross section of a basic AlGaN/GaN HEMT structure is illustrated in Fig.3.6. The semi-insulating GaN buffer layer grown on a SiC substrate provide good electrical isolation between transistors when used in an integrated circuit. The channel region is formed as a two-dimensional electron gas (2DEG) at the interface between the GaN buffer layer and the undoped AlGaN spacer layer [123]. The highly doped AlGaN layer supplies the electrons to the channel. Gate electrode is formed on top of the GaN cap layer. Gate voltage controls the electron density in the channel and thereby the drain-source current.

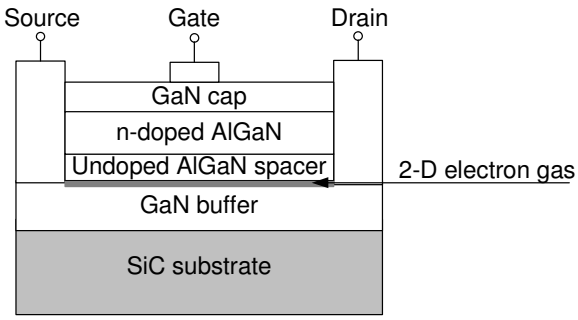

Figure 3.6: Schematic cross section of a basic GaN HEMT structure.

Power MMICs based on GaAs HEMTs are preferably implemented in a via-hole microstrip circuit medium which allows better power handling as compared to the coplanar waveguide (CPW) medium. The via-holes, which primary purpose is to connect the source terminal to DC- and signal-ground, also contribute to the removal of the generated heat to the back-side metallization. The thermal limitations of the coplanar GaAs HEMT amplifiers have been resolved using flip-chip mounting in combination with thermal bumps [26, 124]. On the other hand, excellent thermal conductivity of the SiC substrate enables fabrication of coplanar GaN HEMT power MMICs [31, 32] with comparable power performance to those made in microstrip [33–35].

For the design of X-band PA, a GaN HEMT coplanar MMIC process from Ferdinand Bran Institute für Höchstfrequenztechnik (FBH) has been chosen. Key specifications for the depletion-mode HEMT devices from this process are presented in the Table 3.2. Si3N4 MIM capacitors ($300\ pF/mm^2$) and NiCr resistors ($50\ \Omega/\square$) are available in the process. The MIM capacitors are adapted for high-voltage circuits.

Parameter	*Value*
Gate length $\times$ *Gate width*	$0.35\ \mu m \times 125\ \mu m$
f_t/f_{max}	$23/90\ GHz$
Output power density	$4.4\ W/mm$
$I_{DSS}(@V_{GS} = +2V)$	$1\ A/mm$

Table 3.2: Key specifications for the GaN HEMT from FBH's MMIC process [125].

A model of a power HEMT having eight gate fingers comprising a total periphery of 1 mm has been provided by FBH. The model has been implemented as a symbolic defined device (SDD), an equation-based representation in ADS. In order to check validity of the transistor model under large-signal drive, output-power (P_{OUT}) was measured versus swept input available power (P_{IN}), and compared to those generated by the model under same bias, drive and loading conditions at $8GHz$. Prior to this, a load impedances for maximum P_{OUT} and PAE were determined using a load-pull measurement. In this large-signal measurement, the computer-controlled load-tuner presented a wide range of impedances to the transistor, which photo is shown in Fig.3.7. The common-source connected transistor was biased at the drain-source voltage V_{DS}=$28V$ and gate-source voltage V_{GS}=-$2.8V$. Resulting deep class-AB quiescent drain current was I_D=$80mA$, which is 8% of a drain-source saturation current I_{DSS}. An input power P_{IN}=23 dBm was applied to the input, such that large-signal gain of the optimally loaded transistor was compressed by 1 dB below the small-signal value. On the input side, the transistor was terminated for maximum small-signal gain under the optimal load condition.

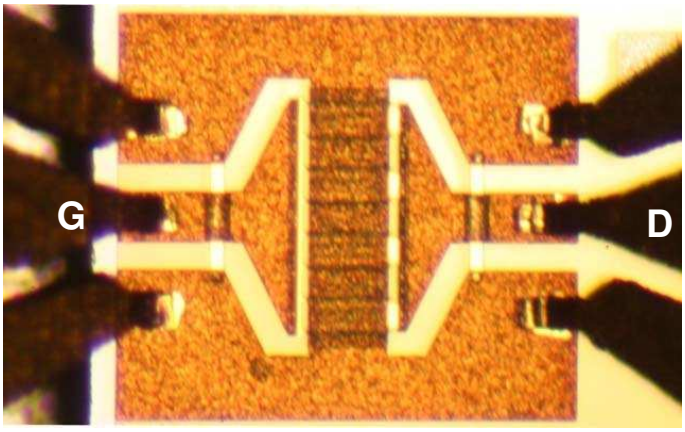

Figure 3.7: An 8×125 μm GaN HEMT connected by probes into a load-pull measurement setup. The interdigitated drain and gate fingers are combined by the drain and gate combining tapers, respectively.

Based on the measured P_{OUT} and PAE values at various load impedances, constant-P_{OUT} and a constant-PAE contours are mapped onto a Smith-chart as displayed in the Fig.3.8. Output power or PAE can be maximized by selecting the corresponding optimum impedance Z_{OPT} as indicated in the figure. Load impedance required for maximum output power in general differs from the impedance maximizing the gain. Since PAE depends not only on the output power but also on the gain, (see eq.(2.2)), the separation between the two Z_{OPT} values is especially pronounced in low-gain devices [126]. The optimum impedance selected for the power-sweep was calculated as an average of the two Z_{OPT} values, i.e.

$$\underline{Z_{OPT}} = 0.5 \times [(15 + j30.9) + (18.9 + j23.2)] \simeq \underline{17 + j27}. \qquad (3.3)$$

Measured and modeled P_{OUT} vs. P_{IN} curves for the transistor biased at 80 mA and terminated by Z_{OPT} calculated for that operating point are displayed in the left plot in Fig.3.9. The right plot in Fig.3.9 displays the compared powers at higher bias current, 190 mA. The model overestimates the saturated output power by around 2 dB under both bias conditions. Lossy et al. [4] have also observed substantial degradation of microwave power compared to the expectations based on DC measurements of FBH GaN HEMTs. This degradation has been ascribed to trapping effects [4].

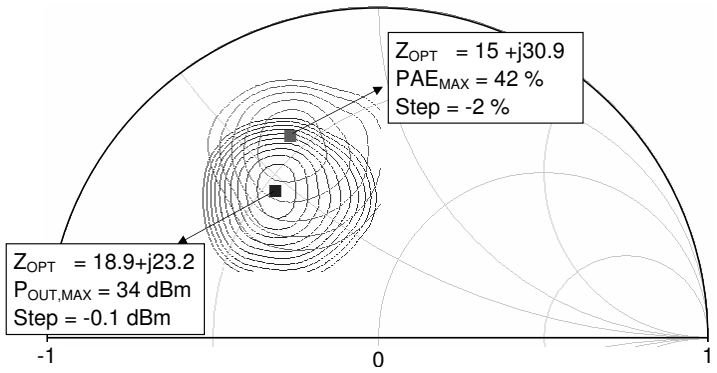

Figure 3.8: Constant output power and constant PAE load-pull contours for the 8-finger device driven by P_{IN}=23dBm and biased at I_D=80mA and V_{DS}=28V.

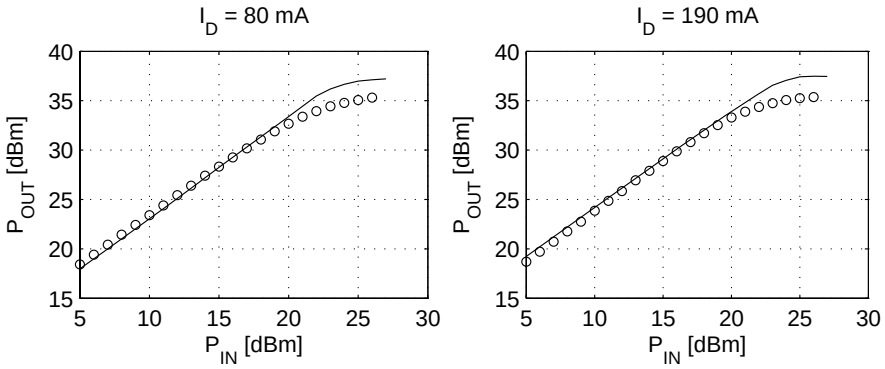

Figure 3.9: Modeled (-) and measured (o) output power vs. available input power for the 8-finger HEMT biased at $28V$ and terminated by 17+j27 load impedance.

The substantial discrepancy between the modeled and measured power performance would not allow characterization of the power amplifier operating under gain compression. Besides the model verification, the presented large-signal measurements will therefore also serve for the design of the amplifier's matching circuits. The model was fortunately capable of reproducing small-signal parameters of the device even at 25 GHz. In order to assess the amplifier performance at various terminations at second harmonic frequency, the model will be exploited at moderate power levels before the onset of the compression. The model parasitics will also serve to find an adequate scaling method for this 8-finger transistor, in order to predict the behavior of a 12-finger transistor used for the PA design.

3.4 HBT Technologies

In a conventional npn homojunction bipolar device (BJT) biased under forward active mode, the electrons injected from emitter into the base diffuse across the base to be finally swept into collector by the strong electric field of the inversely polarized base-collector (B-C) junction [127]. In a heterojunction bipolar transistor (HBT) the emitter is made of semiconductor material having wider bandgap energy compared to the base material. The resulting energy band diagram is reproduced

in the Fig.3.10 [128]. The additional energy barrier ΔE_v appearing in the valence band of the B-E heterojunction increases the current gain $\beta = I_c/I_b$ by making it difficult for the base holes to cross the junction and recombine with the electrons in the emitter. In addition, reduced emitter charge improves the speed. The hole-to-electron current ratio across the heterojunction is given by

$$\left(\frac{I_h}{I_e}\right)_{hetero} = \left(\frac{I_h}{I_e}\right)_{homo} \exp\left(\frac{-\left(\Delta E_g - \Delta E_c\right)}{kT}\right) \tag{3.4}$$

where the factor before the exponential term is the current ratio of an equivalent homojunction, $\Delta E_g = \Delta E_c + \Delta E_v$ is the bandgap difference, ΔE_c is the conduction band discontinuity (spike), k is Boltzmann's constant and T is the temperature. In the abrupt heterojunction ΔE_c impedes the electron injection into the base, which tend to neutralize the advantage of the barrier in the valence band. This spike in AlGaAs/GaAs HBTs can be eliminated by compositional grading of the Al-content in the emitter very close to the interface [129].

Base profile in most HBTs is actually compositionally graded. This causes gradual narrowing of the bandgap towards the collector as illustrated in the Fig.3.10. The created electric drift-field accelerates the electrons, thereby reducing the base transit time. This is another attractive feature of the HBT. Two figures of merit (FOMs) characterizing the high frequency capabilities of the transistors are the unity-current-gain frequency f_t and maximum oscillation frequency f_{max}. In order to illustrate the above-mentioned advantages of the heterojunction effects it is instructive to examine the usual expression for f_t [130] and f_{max} [127],

$$f_t = \frac{1}{2\pi}\left\{\tau_b + \tau_e + \tau_c + \frac{kT}{qI_c}\left(C_{be} + C_{bc}\right)\right\}, \tag{3.5}$$

$$f_{max} = \sqrt{\frac{f_t}{8\pi C_{bc} R_b}}. \tag{3.6}$$

Here τ_b, τ_e and τ_c are electron transit times through base, emitter and collector, respectively, C_{be} and C_{bc} are depletion capacitances of the two junctions and R_b is the base series resistance.

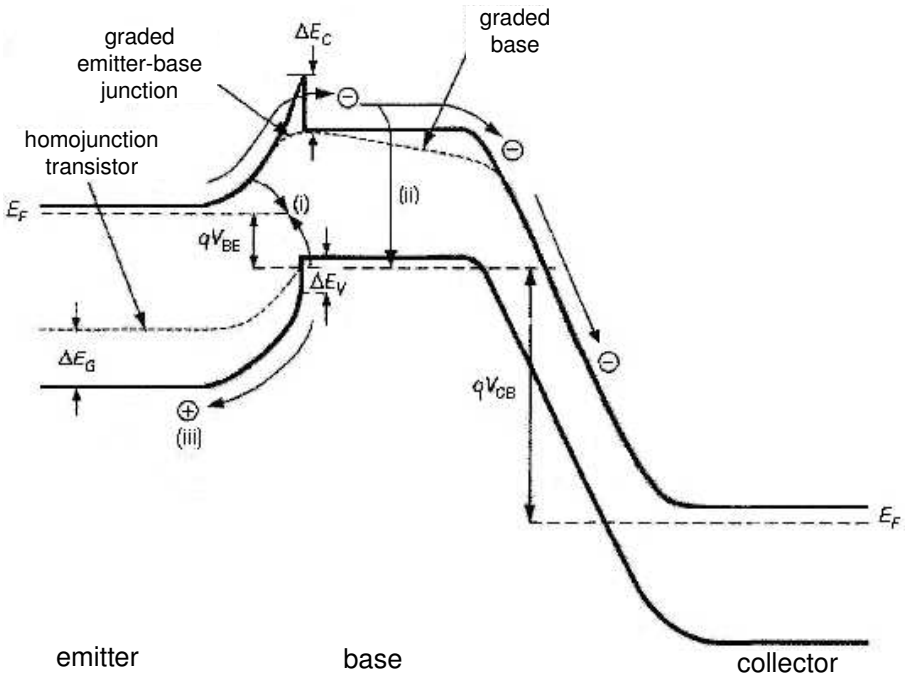

Figure 3.10: Energy band diagram of the HBT biased in forward active mode [128].

Reduction of the τ_b due to the field-aided transport elevates f_t and thereby also f_{max}. Moreover, reduced base hole current in an HBT opens a possibility to either decrease the emitter doping or to increase the base doping, while maintaining high β [131]. The benefits of these two actions are:

- The reduced emitter doping cuts down the C_{be}, which improves both FOMs.
- Increased base doping enhances f_{max} through reduction of R_b.

To take a full advantage of reduced base transit time in a graded-base HBT, collector transit time should be minimized as well, which can be accomplished by increasing a doping in the intrinsic collector. This approach fortunately also postpones the base widening (Kirk-effect) [132] to a higher collector currents, thereby also improving fre-

quency response. An important drawback of high collector doping is reduced breakdown voltage.

3.4.1 InP HBT Technology

InP HBT technology developed by Alcatel-Thales III-V laboratory (ATL) was presented in reference [133–135]. During the last decade, the technology has been used to fabricate high-speed integrated circuits for >40 Gbit/s optical transmission systems [133–137].

The HBT epitaxial structure is grown on semi-insulating InP substrate. It comprises a low-doped $120nm$ InP emitter, and 30-50nm wide InGaAs base with graded indium composition. Doping level in the base is optimized to maintain a low sheet resistance while keeping high current gain. Step-graded collector provides a heterojunction at the B-C interface and gives a high breakdown voltage required for power applications.

The HBTs have emitter length of $1.5\mu m$, and available emitter widths are 3, 6, 10, 15 and 20 μm. Typical performance of the $10 \times 1.5\ \mu m^2$ device are listed in the Table 3.3. For circuit fabrication, transistors are interconnected using vias through polyamide. Three Ti/Au interconnect metal layers, TaN resistors (50 $\Omega/\square$) and MIM capacitors ($0.36\ fF/\mu m^2$) are available. It should be noted that ATL has recently developed a faster, $300GHz$ f_t, process based on reduced emitter length, 0.5 μm [138].

Parameter	*Value*	*Remarks*
β	50	peak value
Peak f_t/f_{max}	$170/170GHz$	@$1.5V$, $1.5mA/\mu m^2$
BV_{CEO}	$7V$	@$100\mu A$
Emitter area	$10 \times 1.5\mu m^2$	

Table 3.3: Key specifications for the ATL's $10\mu m$ InP HBT [133,135].

The design of E-band power amplifier undertaken in this thesis was based on the $10\times1.5\mu m^2$ device. A large-signal UCSD model was provided [11] for use in Agilent ADS. Comparison between the measured and modeled data is summarized in Fig.3.11. The small inaccuracy in f_t fit at $2.5V/20mA$ will possibly introduce slight uncertainty in

the small-signal behavior of the PA, which will be biased near that operating point. Apart from that, the model is capable of accurately describing behavior of the device. Especially, good consistency is observed in the saturation region (low voltage region) of the DC output characteristics, which is of particular importance for prediction of the output power under large-signal drive. The shown S-parameters are taken around peak f_t bias point ($1.6V$, $27mA$) and up to $65GHz$.

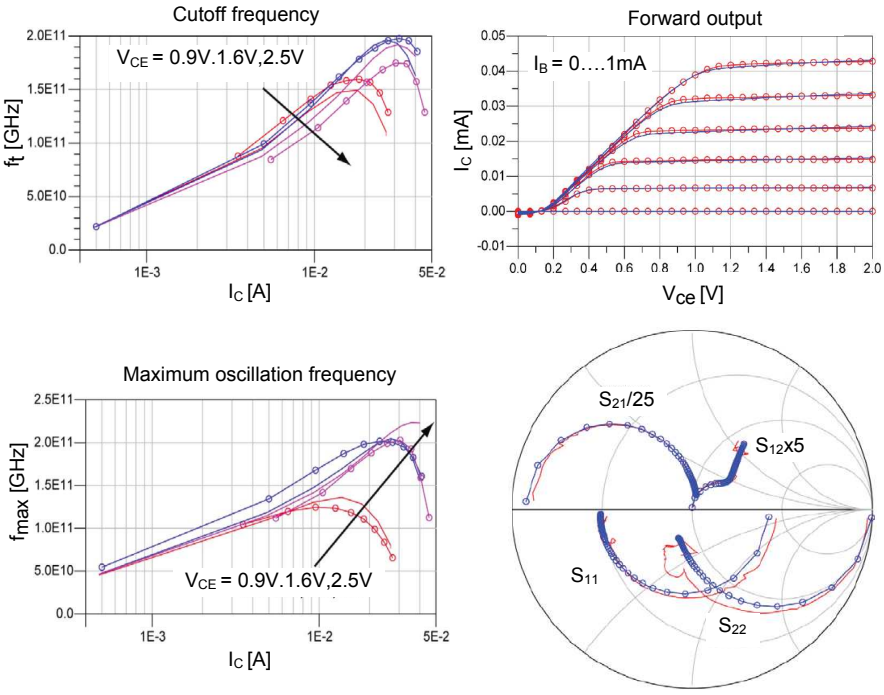

Figure 3.11: Measured (o) versus simulated (-) data for the $1.5\times10\mu m^2$ InP HBT [11].

Another device, used for quadrature oscillator design, has an emitter area of $3\times1.5\mu m^2$. The model provided for this design has been described in [139]. Comparisons between S-parameters, collector-base capacitance and f_t measurements/model reveal globally a good agreement. Large-signal verification of the two InP HBT models has not been performed.

3.4.2 SiGe HBT Technology

In a SiGe based HBT, heterojunctions at base-emitter and base-collector interfaces are formed by addition of germanium (Ge) into the base. Linear increase of Ge concentration from B-E towards the B-C junction provides a gradual narrowing of the bandgap as in the case of the InP HBT. The resulting field-aided transport leads to improved transit time. However, very big improvement is difficult to reach because of the technological need to limit the Ge concentration and/or thickness of the base.

IHP institute provides a BiCMOS process family SG25H that integrates carbon-doped SiGe HBT into an advanced 0.25-μm CMOS platform [140]. Particularly, SG25H2 is a complementary BiCMOS process (CBiCMOS) containing npn devices as well as pnp-type bipolar transistors. This state-of-the-art pnp HBT offers peak f_t/f_{max} values of $90/120GHz$ at $2.8V$ collector-emitter breakdown voltage BV_{CEO}. Device exhibiting highest f_t and f_{max} but lowest breakdown voltage in this process is an npn-type HBT. Key set of electrical parameters for that device are listed in Table 3.4. Model extraction for the SiGe HBT and evaluation of its performance at 73.5 GHz will be described in chapter 5.

Parameter	*Value*	*Remarks*
β	200	@$V_{be} = 0.7V$
peak f_t/f_{max}	170/170 GHz	@$V_{ce} = 1.5V$
BV_{CEO}	1.9 V	
BV_{CBO}	4.5 V	@$I_c = 0.1\mu A$
Emitter area	0.21×0.84 μm^2	

Table 3.4: Key specifications for the npn HBT from the IHP's SG25H2 CBiCMOS process [141].

The schematic cross-section of the npn HBT is shown in Fig.3.12. Highly-doped Si-poly is used to contact intrinsic base and emitter regions resulting in low resistance. Low-resistance of the external subcollector was obtained by high-dose ion implantation and by lateral shrinking of the device dimensions. This is beneficial for power amplifier performance since collector resistance limits the voltage swing

achievable by the device. Low collector resistance also reduces a collector charging time that contributes to the the total transit time, as it will be shown later in eq.(5.43).

Complete lateral enclosure of the collector wells by the shallow trench isolation sidewalls (STI) improves the low-capacitance isolation to the substrate. The absence of deep trench isolation, which is more commonly used in SiGe HBTs [142,143], improves the heat dissipation [144].

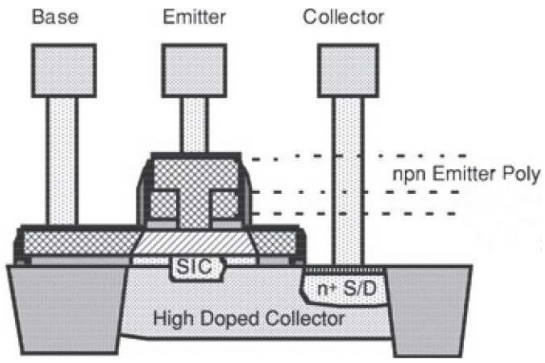

Figure 3.12: Schematic cross-section of the npn HBT structure of the H2 BiCMOS process from IHP [140].

Chapter 4

GaN HEMT X-band Power Amplifier Design

This chapter will present the design of fully monolithic two-stage high-power amplifier based on the coplanar waveguide gallium-nitride HEMT technology described in the section 3.3.

Peak PAE is usually reached at high input drive level, where significant part of the consumed DC-power is converted into a fundamental-tone power being dissipated in the load. On contrary, increasing the drive power also increases the degree of nonlinearity. Efficiency and power capability at high levels of linearity can be improved with appropriate circuit design. The performance of the power amplifier is strongly influenced by the drain bias current I_D of the unit transistor cells. The measurements of the power-transistor performance presented in this chapter will provide a basis for the selection of I_D. Dependence of efficiency and gain on input power will by first evaluated in a one-tone test at different I_D values. The intermodulation distortion of the power device was also measured in a two-tone test with I_D as parameter. Concept of intermodulation distortion, widely adopted FOM of linearity, will be briefly explained. Measurement setup and collected results will be discussed.

Another aspect that needs a careful attention is termination of the devices at higher harmonic frequencies. The harmonic tuning is well-known method of improving the output power and the efficiency of

a power amplifier [145, 146]. The effects of source and load harmonic impedances on the voltage and current waveforms and PAE will be investigated. The study is based on large-signal model simulations. Most favorable harmonic impedances will be identified and approximate values realized in the amplifier circuit.

In the section 3.3, large-signal measurements of the power HEMT with gate pitch 50 μm were discussed. The gate pitch determines outer dimensions of the multi-finger device and thereby generated power per chip area. Hence, power devices with reduced gate pitch and same outer dimensions are desirable. The S-parameters and the optimum load impedance of a 33μm-pitch device will be obtained by scaling the measured data of the 50μm-pitch device presented in the section 3.3.

The driver stage of the power amplifier consumes the supply power without contributing to the useful output power. It is therefore not surprising that the two most efficient GaN MMIC results, 44% [31] and 35.3% [34], presented previously in the Fig.3.1, contain only one amplifier stage. Considerations regarding the optimum driver periphery will be discussed. The amplifier topology and details of the circuit will be presented. Finally, the amplifier performance will be estimated.

4.1 Bias-Current Selection

The available voltage region of a field-effect transistor spans from the knee region where I_D begins to saturate up to the break-down voltage on the I_D/V_{DS} characteristics. In order to obtain a high output voltage swing and resulting high output power, FBH devices are normally biased at 28 V drain-source voltage [31, 147]. The 28 V bias voltage was adopted in this work. In this section, the drain bias current providing most favorable compromise between efficiency and linearity performance of the used power HEMTs will be identified. One-tone measurements at various bias currents will provide information about gain and PAE versus swept input power. Two-tone measurements will provide a basic insight into intermodulation distortion behavior of the transistor.

4.1.1 One-Tone PAE and Gain Considerations

The large-signal measurement described in section 3.3 was made to check validity of the 8-finger transistor model. Same test was made to compare the performance of the transistor when biased at 20 mA, 80 mA, and 190 mA, respectively. The collected measurement results are presented in the Fig.4.1.

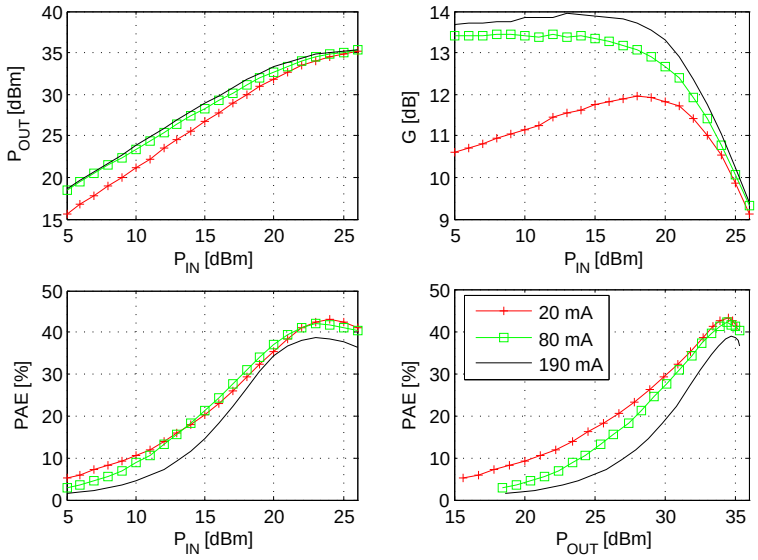

Figure 4.1: One-tone performance of the 8×125μm HEMT biased at 28 V and three different drain currents. The measurements were taken at 8 GHz.

The 20 mA solution can be considered as class-B operating point, since the device is biased at the threshold voltage, $V_{GS} = -3.3V$. The transducer gain G in that mode of operation expands substantially with the available generator power P_{IN}, as depicted in the figure. This is mainly caused by the slope of the nonlinear transfer characteristic $(\partial I_D/\partial V_{GS})$, which starts increasing with the V_{GS} above the threshold voltage. This slope is known as a small-signal transconductance g_m.

The 80mA deep class-AB solution exhibits more constant G-P_{IN} relationship, remarkably higher small-signal gain, and similar PAE at higher power levels, as compared to the 20mA solution. Around peak PAE the gain difference is, however, less pronounced.

The gain can be only slightly improved if the drain current is further increased to 190 mA. At the same time, the 190 mA solution exhibits inferior PAE performance, as demonstrated in the two bottom plots of Fig.4.1. This is especially pronounced at moderate and lower power levels, since high bias current is flowing through the device regardless of the applied P_{IN} or output power P_{OUT}.

From the discussion above it can be concluded that low bias currents, 20 and 80mA, provides more favorable compromise between high gain and high PAE performance, as compared to the 190 mA current.

4.1.2 Intermodulation Distortion

An amplitude modulated carrier signal gets spectral components stemming from the baseband signal below and above the carrier frequency [148]. When the carrier is suppressed the equation for such signal reads

$$V_{IN} = C\left[\cos\omega_A t + \cos\omega_B t\right]. \tag{4.1}$$

In this example, $(\omega_A - \omega_B)$ is the angular frequency of the baseband signal modulating the carrier at the center frequency $(\omega_A + \omega_B)/2$. Time-domain waveform of the two-tone signal at the input of a device is illustrated in the Fig.4.2.

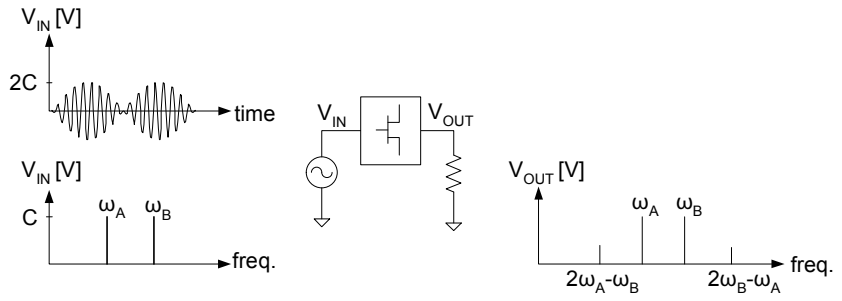

Figure 4.2: Two-tone time domain voltage waveform and frequency components at input and output of a power amplifier.

Being a nonlinear circuit, a power amplifier driven by the two-tone signal generates additional frequency components. The third order intermodulation products (IM3) at sideband frequencies $(2\omega_A - \omega_B)$

and $(2\omega_B - \omega_A)$ [149] are of particular interest for communication systems since they cause bit error rate degradation [150]. The frequency spectra at the amplifier output is indicated in the Fig.4.2. Third order intermodulation distortion (IMD3) is often used as a linearity measure of a PA. It is defined as a ratio between the single-carrier output power (either at ω_A or at ω_B) to the power of the single IM3 product.

Two-Tone Measurement Setup

Two-tone measurements were carried out to understand basic linearity characteristics of the 8-finger power HEMT biased at three different currents. The intermodulation distortion was measured in the two-tone test setup illustrated in Fig.4.3. The spectral contents at the device output were monitored by the Agilent Performance Spectrum Analyzer (PSA). The test signal composed of two tones separated by 10 MHz around 2 GHz was generated by the Agilent Performance Signal Generator (PSG). To obtain sufficient drive level the signal was subsequently amplified by the power amplifier (PA), which unfortunately also generated its own IM3 products. Cancelation of these frequency components required predistortion of the PSG signal. This linearization of the PA output was carried out using the Agilent Signal Studio software installed on the PC. In the calibration process the software collected the distortion data from the Performance Spectrum Analyzer (PSA) driven by the PA and iteratively computed a parameter controlling the predistortion of the PSG.

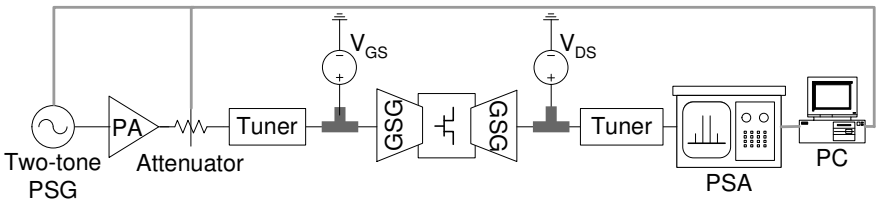

Figure 4.3: Two-tone measurement setup.

Input power sweep was realized through the computer controlled attenuator as indicated. Thus the PA was driven at constant power level, and a single predistortion parameter was valid across the entire

power range. The mechanical tuners applied at the transistor input and output provided maximum gain and maximum output power, respectively. The transistor was mounted on a copper flange. It was connected to the power supplies through the bias-Ts as illustrated. Losses in the measurement equipment at the device output were subtracted from the measured results.

Two-Tone Measurement Results

The intermodulation distortion data monitored on the PSA are plotted in the Fig.4.4. Most linear operation was exhibited at highest bias current 190 mA under low-power operation, since the device operated at most linear part of the I_D-V_{GS} characteristic.

At higher power range, low bias currents tend to provide lowest IMD3 as indicated. As the bias current reduces from the 190 mA, a 'valley' start to appear in the IMD3 plot at high-power levels. The occurrence of the high-power 'valley' in the vicinity of the class-B bias point has also been observed by other authors [151–153]. This property of HEMT devices has been analyzed and explained as opposite phase interactions of various intermodulation products [153].

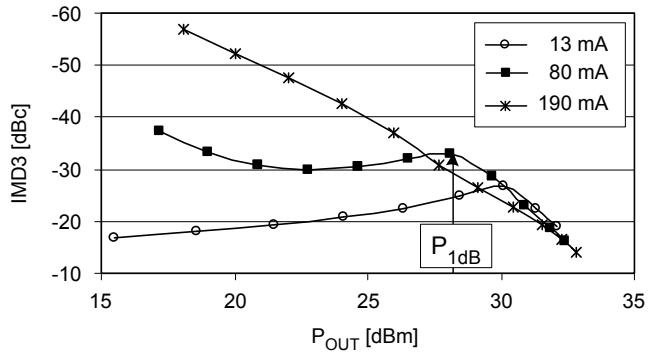

Figure 4.4: Measured IMD3 versus output power (each carrier) for a $1mm$ HEMT at $2GHZ$ center frequency, $10MHz$ tone spacing and V_{DS}=$28V$.

As suggested by the curves in the Fig.4.4, a penalty of reducing the current below $80mA$ could be an excessive distortion. Data-sheets for commercial solid-state [154–156] and TWT [157] high-power amplifiers

for satellite uplink applications in the 7.9-8.4GHz band, often report intermodulation distortion of -25 dBc. As it appears in the Fig.4.4, as the current is reduced from 190 to 80 mA, the point where IMD3 falls to -25 dBc is pushed up 1 dB on the P_{OUT} scale.

In the single tone measurements presented in the Fig.4.1, the 1mm device, biased at 80 mA, reached 1dB gain compression at output power of 33.4 dBm. When excited by two tones, the device reached 1dB compression at around 28dBm, that is, almost 6dB lower output power for each carrier. This power level is indicated as P_{1dB} in the Fig.4.4. According to the figure, at the power levels above 27 dBm (1dB back-off), the 80mA operating point provides best linearity. At the same time, for any power level up to 29dBm (2dB compression point) the IMD3 is better than -30 dBc.

The 80mA/mm current results in improved linearity at high power levels. Limitations in the setup allowed the measurements to be done only up to 2 GHz, which is fairly below the 8 GHz where the transistors will operate in the amplifier. As mentioned, however, the other groups have observed similar IMD3 behavior of GaN HEMTs biased near class-B. This bias condition also offered high gain and high PAE in the one-tone measurements. It was therefore decided to adopt the 80mA/mm operating condition for the transistors used in this MMIC design.

4.2 Device Scaling

A HEMT device with reduced pitch and unchanged number of gate fingers exhibits reduced outer width, which saves the chip area. Apart from being cost-effective, such a solution requires an output combining network with reduced line length and consequently lower power loss and higher efficiency. The 8-finger device discussed until now exhibits 50μm gate-to-gate spacing (gate pitch). Another available device had 12 gate fingers, 33μm gate pitch, and same dimensions of the tapers combining the gate and drain fingers, as the 8-finger device (see Fig.3.7). Thanks to the larger total periphery, this device offered increased output power at same chip size for the designed PA.

S-parameters and load-pull measurements of the 12-finger/33μm HEMT were not available. Scaling the 8-finger device data was therefore attempted. An appropriate scaling trend was derived by comparing the measured S-parameters of 12-finger and 18-finger devices having a gate pitch 50 and 33 μm, respectively. The outer device width of these two devices was 50% larger as compared to the width of the 8-finger device. The 18-finger device generated about 1.8 dB (or $\sim$1.5$\times$) higher power than the 12-finger device due to the 50% larger periphery. Similar improvement was therefore expected from the attempted 8-to-12 finger scaling.

4.2.1 Scaling Method

Equivalent circuit showing parasitic elements of the transistor structure is depicted in Fig.4.5 (left). Values of the passive elements taken from the device model are summarized in Table 4.1. Elements C_{TG}, L_{TG}, and C_{TD}, L_{TD} represent the parasitic effects of the two tapers connected to the gate and drain side, respectively. Fig.4.5 (right) illustrates schematic cross section of the HEMT interdigitated structure including the gate and drain fingers as well as the airbridge connecting the source fingers. The effective airbridge inductance L_S was assumed not to scale, since the airbridge length was unchanged.

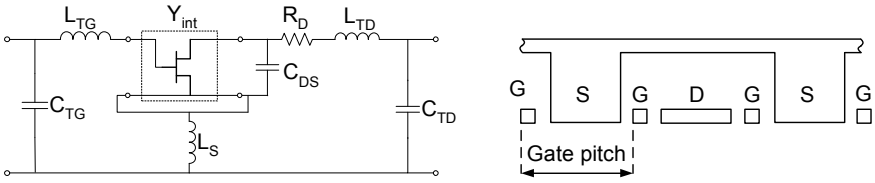

Figure 4.5: Left: Equivalent circuit of the HEMT including the taper parasitics. Right: part of a schematic cross section showing gate, source and drain fingers.

A 4-step procedure for scaling the 12-finger to the 18-finger device was carried out by optimizing R_D and C_{DS} values as described below. The R_D and C_{DS} were optimized to fit the scaled and measured S-parameters of the 18-finger device. Increasing the number of the gate fingers by the scaling factor 1.5 (=18/12) while keeping the

total device width and finger spacing constant, slightly reduces the total width of the drain fingers. The total drain access resistance R_D is therefore expected to increase in stead of being reduced 1.5 times. The scaling trend is less obvious for the drain source capacitance C_{DS}, since the total drain area and associated parallel plate capacitance to the airbridge diminish, but the total fringing capacitance increases due to the increased number of drain fingers.

Step 1: A small-signal admittance matrix $Y_{int,12}$ representing the intrinsic 12-finger HEMT device was firstly calculated by subtracting the contributions of the passive elements to the measured Y-parameter matrix of the entire device, $Y_{meas,12}$. The calculation was accomplished through the eq.(4.2-4.5).

$$Y_{d1} = Y_{meas,12} - \begin{bmatrix} j\omega C_{TG} & 0 \\ 0 & j\omega C_{TD} \end{bmatrix} \tag{4.2}$$

$$Y_{d2} = \left\{ Y_{d1}^{-1} - \begin{bmatrix} j\omega L_{TG} & 0 \\ 0 & R_D + j\omega L_{TD} \end{bmatrix} \right\}^{-1} \tag{4.3}$$

$$Y_{d3} = Y_{d2} - \begin{bmatrix} 0 & 0 \\ 0 & j\omega C_{DS} \end{bmatrix} \tag{4.4}$$

$$Y_{int,12} = \left[Y_{d3}^{-1} - j\omega L_S \right]^{-1}. \tag{4.5}$$

.

Step 2: Intrinsic admittance matrix of the 18-finger device was then calculated by linear scaling as $Y_{int,18}$=1.5×$Y_{int,12}$.

Step 3: The elements C_{DS}, and R_D of the 18-finger device were scaled using the optimization factors k_C and k_R as

$$C_{DS,18} = k_C C_{DS,12} \tag{4.6}$$

$$R_{D,18} = k_R R_{D,12}. \tag{4.7}$$

Step 4: Finally, the admittance matrix of the 18-finger device was calculated by attaching $C_{DS,18}$ and $R_{D,18}$, as well as the remaining non-scaled passives of the structure in the Fig.4.5 to the $Y_{int,18}$.

By optimization of the empirical factors k_C and k_R the modeled S-parameters of the entire 18-finger device were fitted to the measured ones. The most representative values were found to be $k_C = 1.25$, and $k_R = 1.07$. The scaled parasitic drain resistance increased slightly, as expected. Note that, if the gate-pitch reduction was disregarded in the scaling procedure, and only the number of fingers was considered, the two scaling factors would equal 1.5 and 1/1.5, respectively.

Good agreement was obtained between the scaled and the measured S-parameters of the 18-finger device. Most apparent discrepancy was observed in the S_{22} magnitude, which was highly dependent on C_{DS} and R_D elements. In Fig.4.6, the 'Simple 1.5× scaling' curve represents the intrinsic device scaled 1.5 times, inclusive C_{DS} and R_D. Using the 'Correct scaling' method described above, the agreement between the measured and the modeled $|S_{22}|$ improves. Slight improvement was also observed in $|S_{12}|$ fit (not shown).

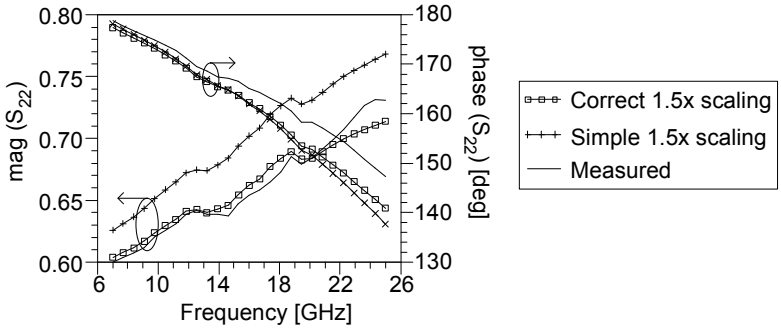

Figure 4.6: Measured and modeled S22 for the 8-finger device.

Fingers / Pitch	C_{TG} $[fF]$	L_{TG} $[pH]$	C_{TD} $[fF]$	L_{TD} $[pH]$	R_D $[\Omega]$	C_{DS} $[fF]$	L_S $[pH]$
12 / 50 μm (not scaled)	121	134	121	130	1.14	362	7.6
8 / 50 μm (not scaled)	91	126	91	123	1.54	250	2.2
12 / 33 μm (scaled)	91	126	91	123	1.44	312	2.2

Table 4.1: Parasitic element values for the GaN HEMTs.

4.2.2 Results of the Scaling

Finally, using the scaling method with k_C and k_R calculated above, S-parameter matrix of the 12-finger device with $33\mu m$ pitch was predicted by scaling the 8-finger device with $50\mu m$ pitch. The obtained C_{DS} and R_D are presented in the Table 4.1.

Optimum load impedance of the 8-finger HEMT, $Z_{OPT} = 17 + j27$ Ω, found in the load-pull measurement described in section 3.3, was scaled in the same manner to obtain Z_{OPT} of the 12-finger/$33\mu m$ device. The optimum impedance at 8 GHz became $\underline{13 + j17}$ Ω.

4.3 Second-Harmonic Tuning

High efficiency power amplifier design requires proper device termination not only at fundamental frequency but also at higher order harmonics. By applying adequate harmonic terminations, the output voltage and current waveforms can be shaped such that the power dissipated in the device is minimized. Aiming at high efficiency, harmonically tuned linear microwave SSPAs often employ lowest possible load impedance at second harmonic [146, 158–160]. This at the same time reduces the harmonic level at the output, and prevents the dissipation of the 2^{nd} harmonic energy in the load.

An ideal parallel-tuned amplifier provides a short for higher order harmonics at the output. This results in a sinusoidal drain-source voltage and puls-shaped drain-current [161]. Theoretical limit for the drain efficiency of a parallel tuned amplifier biased in class-B is 78.5%, before the onset of the current clipping. A fully monolithic 5-6GHz GaAs FET amplifier showed 70% PAE [146]. Low output impedances were realized at both 2^{nd} and 3^{rd} harmonics using a short-circuited microstrip stubs near the transistor drain.

An important aspect concerning harmonic tuning approach is the generator impedance presented to the gate at higher harmonics. The effect of input harmonic terminations on GaAs based power-pHEMT performance at 5 GHz have been investigated in [162]. It has been found that the non-linear effect of C_{GS} can distort the driving voltage waveform and in turn the ideally half-sinusoidal output current

waveform, resulting in a greatly reduced efficiency. The problem has been resolved by application of a short-circuit input harmonic termination [162]. Same approach for enhancing the efficiency has been successfully applied in a design of PA MMIC exhibiting 8 W and 50% efficiency at C-band [163], and it has been also suggested by other research groups [164,165]. Despite of that, some authors have ignored this aspect of the amplifier design and exclusively considered the load harmonic manipulation [166,167].

In this work, manipulation of the 2^{nd} harmonic load and generator impedances was carried out aiming at efficiency enhancement of the 12-finger HEMTs used in the output stage. Identification of the favorable and unfavorable harmonic terminations was carried out using the non-linear device model and Harmonic Balance simulation tool provided by Agilent ADS software.

Principal circuit diagram of the simulated $1.5mm$ HEMT including the taper parasitics is illustrated in the Fig.4.7. The device was biased at the selected current density of 80 mA/mm and drain-source voltage 28 V. At the fundamental frequency the device was terminated by the scaled optimum load impedance $Z_{OPT} = 13 + j17\,\Omega$, and generator impedance, $1.4 - j2\,\Omega$, required for maximum gain.

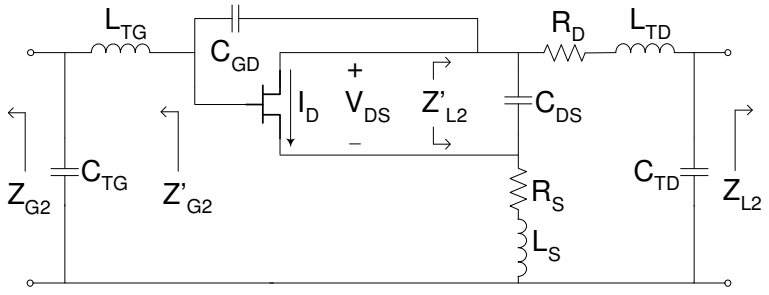

Figure 4.7: Equivalent representation of the intrinsic 12-finger HEMT ($33\mu m$ gate-pitch) including the parasitic elements, and indicating second harmonic impedances.

4.3.1 Parallel-Tuning Case: Shorted Second Harmonic

As a starting point for the investigation, the generator impedance $Z_{G2} = -j14\ \Omega$ and the load impedance $Z_{L2} = -j15\ \Omega$ were applied at the second harmonic frequency 16 GHz. The chosen Z_{G2} provides short-circuit seen from the intrinsic gate terminal, i.e. $Z'_{G2} = 0$. The chosen Z_{L2} assures low impedance across the drain-source terminals of the intrinsic device, $Z'_{L2} = 2\Omega$. This is only an approximation to the short circuit, due to the finite source and drain resistances, R_S and R_D, respectively. The two resistors actually dissipate around 11% of the total fundamental output power P_{OUT}. In an ideal parallel tuned amplifier this would cause the drain efficiency to drop from 78.5% to around 70%.

Simulation was performed at 8 GHz and 20 dBm input power yielding P_{OUT} of 33.2 dBm. This power corresponds to $2dB$ output back-off[1], when the measured P_{1dB} is taken as the reference. Fig.4.8 shows the load trajectory and time waveforms of the intrinsic drain-source voltage V_{DS} and the intrinsic drain current I_D. Second harmonic control constrains the output voltage to by nearly a sinusoid at the fundamental frequency. Current pulses occur at the instants where the voltage is low, as required by the high-efficiency concept.

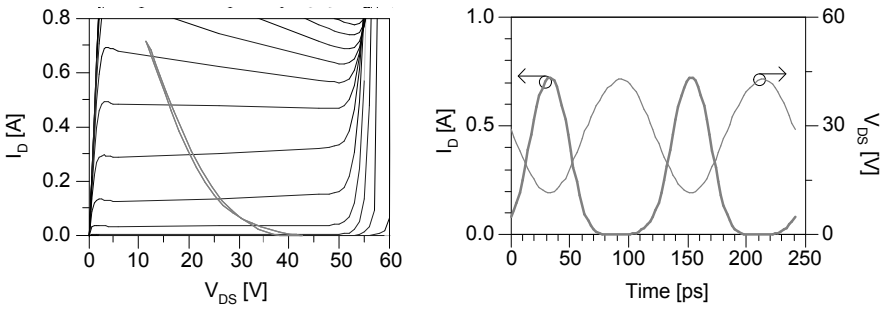

Figure 4.8: Parallel tuned intrinsic HEMT terminated by $Z_{G2} = -j14\ \Omega$ and $Z_{L2} = -j15\ \Omega$ at the extrinsic gate and drain, respectively. Left: load trajectory. Right: time-domain waveforms. V_{DS} and I_D are indicated in the Fig.4.7.

[1]The $2dB$ output back-off refers to the P_{OUT} which is 2 dB below the P_{OUT} in $1dB$ compression.

4.3.2 Impact of Third and Higher Order Harmonics

In this work, second harmonic control of the generator and the load impedance was performed. The 3$^{\text{rd}}$ and higher order harmonics were not considered due to the reasons explained below. They were terminated by 50 Ω in all the presented simulations.

In the parallel tuned amplifier described above, the 3$^{\text{rd}}$ harmonic content of I_D stayed at least 17 dB below the 2$^{\text{nd}}$ harmonic at fundamental power levels ranging up to $2dB$ output back-off. Consequently, the voltage and current waveform shapes were mostly dependent on the 2$^{\text{nd}}$ harmonic terminations. By modification of the generator and load impedances at 3$^{\text{rd}}$ harmonic frequency, only a small change in PAE was observed, ±0.7%.

The 3$^{\text{rd}}$ harmonic tuning became increasingly important as Z_{G2} and Z_{L2} moved away from the values required for parallel tuning. However, up to the $2dB$ back-off it was not possible to obtain higher PAE than that obtained by shorting the 2$^{\text{nd}}$ harmonic.

At higher power, beyond $2dB$ compression level, larger change in PAE (up to ±2.8%), was possible due to rapid increase of 3$^{\text{rd}}$ harmonic content of the drain current. Creation of an open circuit for the 3$^{\text{rd}}$ harmonic at the intrinsic device terminals is actually a way to a class-F operation [168]. Second harmonic is shorted as in the parallel-tuning case. Taking the advantage of a square-like V_{DS} waveform, class-F tuning offers larger P_{OUT} and PAE as compared to the parallel-tuning case. Since the class-F operation required significant gain compression to generate the 3$^{\text{rd}}$ harmonic output current, the intermodulation distortion would have degraded. Moreover, the model inaccuracy in the compression regime would not allow reliable harmonic control.

Finally it should be mentioned that the 4$^{\text{th}}$ and 5$^{\text{th}}$ harmonics had even less impact on the PAE as compared to the 3$^{\text{rd}}$ harmonic.

4.3.3 Other important Cases

Conclusions presented in following were drawn while tuning the 2$^{\text{nd}}$ harmonic impedances Z_{G2} and Z_{L2} around the two start-values determined in the parallel tuning approach, as described above. Again, the results are based on the input power level of 20 dBm.

- Z_{G2} values in the vicinity of $-j14\,\Omega$ assuring nearly a short circuit seen by the transistor gate indeed maximize the PAE. The exact optimum value of Z_{G2} actually ranged between $-j12\Omega$ and $-j16\,\Omega$, depending on the chosen Z_{L2}.

- Generator second harmonic impedance value of $-j6\,\Omega$ tunes out the input capacitance at 2^{nd} harmonic frequency. Resulting V_{GS} waveform gets distorted and I_D pulses broaden as depicted in the Fig.4.9 (left plot). This causes excessive power consumption in the device and deteriorates the PAE. Fig.4.10 illustrates the load trajectory and PAE simulated for this case, denoted as 'Worst Z_{G2}'. Load impedance Z_{L2} was kept at the original value for parallel-tuning, $-j15\,\Omega$. As it appears from the Fig.4.10 (right plot), the efficiency is highly dependent on the second harmonic impedance at the transistor input.

- The PAE degradation is also caused by small positive values of Z_{L2}, which tend to tune out the capacitive load presented at the intrinsic device output. The case denoted as 'Worst Z_{L2}' in the Fig.4.9 (middle plot) and Fig.4.10 corresponds to Z_{L2} of $j7\,\Omega$, while Z_{G2} was kept at the original value, $-j14\,\Omega$, used in the parallel tuning example above. Load impedance Z'_{L2} seen by the intrinsic transistor becomes high and real, around $100\,\Omega$, and introduces strong 2^{nd} harmonic component in the V_{DS}. This component is 90° out of phase with the fundamental one.

- On the other hand, moving the Z_{L2} reactance in a negative direction from the start value of $-j15$ would not tune out the capacitive output impedance. This direction of change is therefore expected to be less detrimental. In fact, an improvement of 1.5% in PAE was obtained as Z_{L2} moved towards $-j\infty\,\Omega$. In this case Z'_{L2} changed from $2\,\Omega$ to $(1-j14)\,\Omega$. The shape of the load trajectory for that solution, denoted as 'Optimum' in the Fig.4.10 (left plot), somewhat approximates that of the parallel tuned amplifier.

  Obviously, the lowest possible $|Z'_{L2}|$ $(2\,\Omega)$ does not maximize the efficiency of the investigated GaN HEMT. This is believed to be

caused by the parasitic effects in the transistor. Namely, when C_{GD} and R_D were set to zero, and optimization was repeated, the optimum impedance Z'_{L2} moved back near 0 Ω. The shift of the optimum Z'_{L2} towards negative reactive values does not seem to be caused by the 3rd and higher order harmonics.

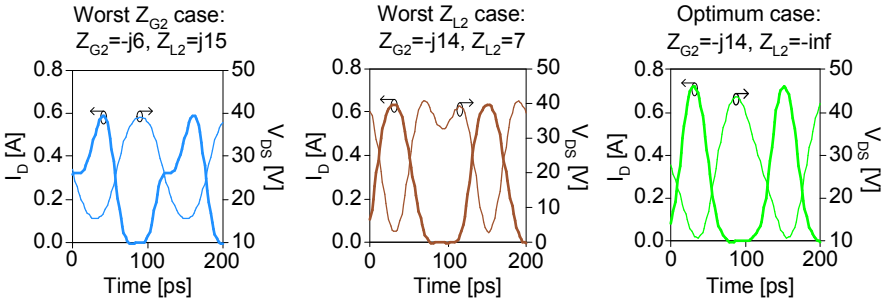

Figure 4.9: Time domain waveforms of the intrinsic device at three different 2nd harmonic terminations and P_{IN}=20dBm.

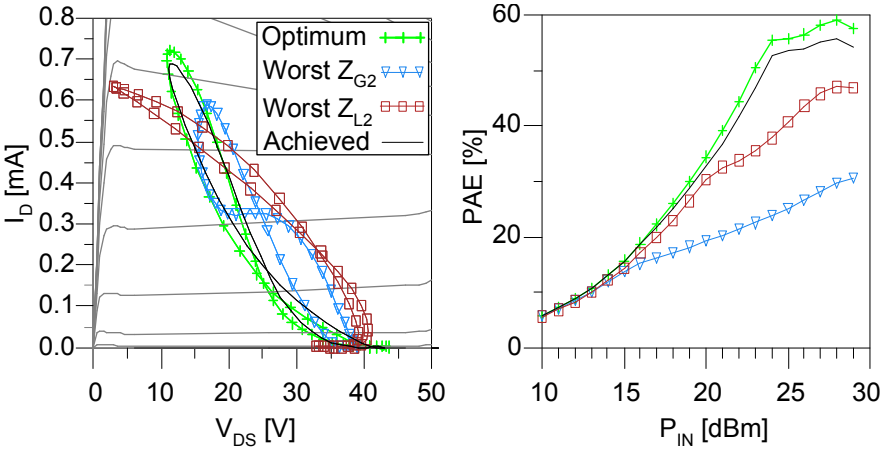

Figure 4.10: Simulated results for various 2nd harmonic terminations providing optimum and worst PAE together with the achieved result. Left: Load trajectories at P_{IN}=20dBm Right: Power added efficiency versus input power.

Presence of the C_{DS} and C_{GD} at the intrinsic drain significantly simplifies implementation of the harmonic load. In high-power mi-

crowave amplifiers employing large-periphery GaN HEMTs, very low 2^{nd} harmonic load impedance can otherwise be difficult to realize because of the losses in the matching circuits [167]. Beneficial effect of a large C_{DS} providing low reactance for the harmonics is well-known [169]. Serious drawback of an excessive C_{DS} is that the 50Ω load needs to be transformed to a low optimum load impedance at the fundamental frequency. This increases the loss in the matching circuit and impedes the wideband operation [169]. Moreover, bandwidth reduction also arises from the fact that the C_{DS} increases the quality factor Q of the transistor output impedance. In fact, higher-Q circuits are intrinsically harder to match then are lower-Q circuits [120]. Simulations of the transistor circuit from the Fig.4.7 reveal however that C_{GD} also have a pronounced effect on the fundamental load impedance. Namely, the optimal impedance $(13+j17)\,\Omega$ transformed back through the drain taper and C_{DS} is found to be $(33+j23)\,\Omega$. The optimum impedance seen by the intrinsic device, however, is real and relatively high, $53\,\Omega$.

4.3.4 Realized Second Harmonic Impedances

The achieved second harmonic impedances and PAE for the four transistors in the output stage are as presented in following.

Load 2^{nd} harmonic impedance, Z_{L2}

As mentioned before, the optimum second harmonic impedance presented to the drain terminal turned out to be $-j\infty\,\Omega$. In fact, any sufficiently high $|Z_{L2}|$ would have similar effect on the transistor efficiency. In the realized power amplifier presented later in this chapter, the achieved Z_{L2} seen from the device output became $\underline{(100+j290)\,\Omega}$.

Source 2^{nd} harmonic impedance, Z_{S2}

The results presented in the Fig.4.10 reveal that the input side of the transistor is even more critical then the load side with respect to 2^{nd} harmonic manipulation. Low 2^{nd} harmonic impedance presented to the intrinsic gate, also implies a low real part of the Z'_{G2}. As

mentioned, the optimal and undesirable reactances are $-j16\ \Omega$ and $-j6\ \Omega$, respectively. The achieved Z_{G2} was $(3-j19)\ \Omega$, providing a $j3\Omega$ additional safety margin for the generator reactance. The intrinsic Z'_{G2} became $(2.5-j3)\ \Omega$.

Simulated results for this achieved combination of Z_{G2} and Z_{L2} are denoted as 'Achieved' in the Fig.4.10. The load trajectory and PAE approximate the 'Optimum' curves.

4.4 Circuit Design

Block-diagram of the designed two-stage power amplifier is illustrated in Fig.4.11. The unit-cell transistors were biased in deep class-AB current density of 80 mA/mm, where high efficiency and low IMD3 were measured. Drain and gate bias voltages are $V_{DD1} = V_{DD2} = 28V$ and $V_{GG1} = V_{GG2} = -2.8V$, respectively. Output matching network serves to combine the output signal of the power stage transistors. At the same time it provides optimum load impedance to these transistors. Similarly, the interstage matching circuit transforms the input impedance of the power stage HEMTs into the optimum load impedance for the driver transistor. It also serves to distribute the driver output signal equally among the power stage transistors. Input matching circuit transforms the input impedance of the driver transistor to the 50Ω generator for minimum return loss. Aiming at high PAE, the output and interstage matching circuits provide the nearly-optimal 2^{nd} harmonic impedances to the power stage transistors, as mentioned in the section 4.3.4.

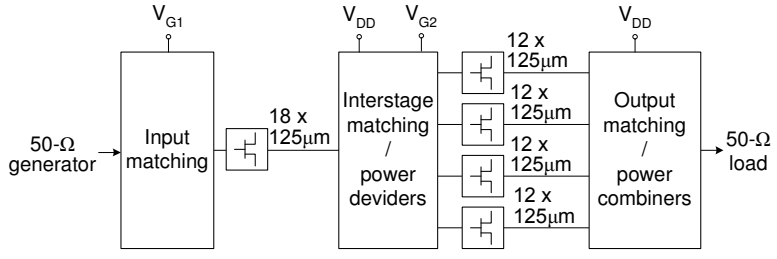

Figure 4.11: Principal block diagram of the realized power amplifier.

Premature saturation of the driver HEMT could limit the output power and also cause a distortion. To avoid this, the driver output periphery should be sufficiently large. Unfortunately, very large driver transistor consumes excessive DC power resulting in reduced PAE. Ratio between the driver periphery (18 fingers) to the periphery of the power stage (48 fingers) is 1/2.7, according to the number of fingers indicated in the Fig.4.11. State-of-the-art GaN HEMT monolithic X-band power amplifiers [31–36, 170, 171] exhibit periphery ratios between 1/4.5 and 1/2. From this point of view, the chosen periphery ratio, 1/2.7, can be considered as 'non-aggressive'. It will be shown in section 4.5 that the driver stage operates in $\sim 5.6dB$ output back-off while the power stage is in $1dB$ compression. This assures linear performance and provides a safety margin for the driver. If the 12-finger driver was used in stead, the periphery ratio would have been 1/4, and the driver back-off would have dropped to $3.9dB$. The predicted PAE would have increased from 29.2% to 30.4%, according to the estimation described in section 4.5.

Diagram and layout of the amplifier circuit are shown in Fig.4.12 and Fig.4.13, respectively. Component values are summarized in the Appendix A. The size of the submitted chip, $3{\times}4mm^2$, is in the range of the state-of-the-art solutions [32–35].

Coplanar transmission lines of the matching/combining networks are represented by the thick lines in the circuit diagram. The drain current is supplied through the stubs, which electrical length is around 45° at 8 GHz. Since the stubs are AC-shorted by the decoupling capacitors, they act as shunting inductors in the matching circuits. The shunting capacitors C_{12}, C_{14} and C_{17}, however, are most important for the impedance transformation. The C_2 capacitor placed close to the input of each power stage transistor provides nearly the optimum second harmonic impedance to these transistors, which eases the optimization of the interstage matching circuit elements.

High device gain at low frequencies necessitates use of the resistive loading in the circuit to prevent parasitic oscillations. Rollet's stability factor K of the amplifier stages devices are lower than 1 around $3GHz$, which implies potential instability [172]. Series connected resistor and capacitor between gate and drain eliminates this problem.

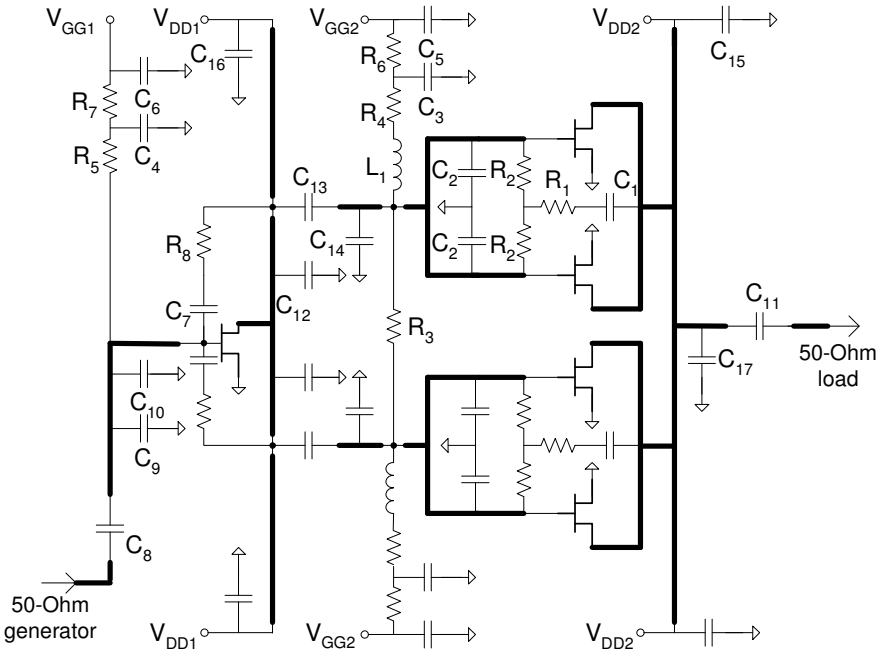

Figure 4.12: Circuit diagram of the power amplifier. Component values are identical in the two circuit half-parts symmetrical around horizontal center axis.

Input impedance of the optimally matched driver transistor is only $(1.4+j4)\,\Omega$. This impedance has to be transformed to $50\,\Omega$ for minimum input return loss. As mentioned earlier, a high transformation ratio hampers the design of wideband matching circuits. Output impedances of the devices are order of magnitude higher as compared to their input impedances. The total amplifier bandwidth is therefore mainly determined by the input and interstage matching circuits rather than the output matching circuit. By introducing losses in the two matching circuits, the amplifier's $1dB$ bandwidth was extended from around 250 MHz to 500 MHz. Resistor R_5 terminated by the decoupling capacitor C_4 in the gate biasing path of the driver transistor dissipates the signal power at the fundamental frequency. Amplifier's power gain reduces around $2dB$ due to the action of the R_5. Same approach was applied in the interstage matching network, where gain reduction due to R_4 was 1 dB.

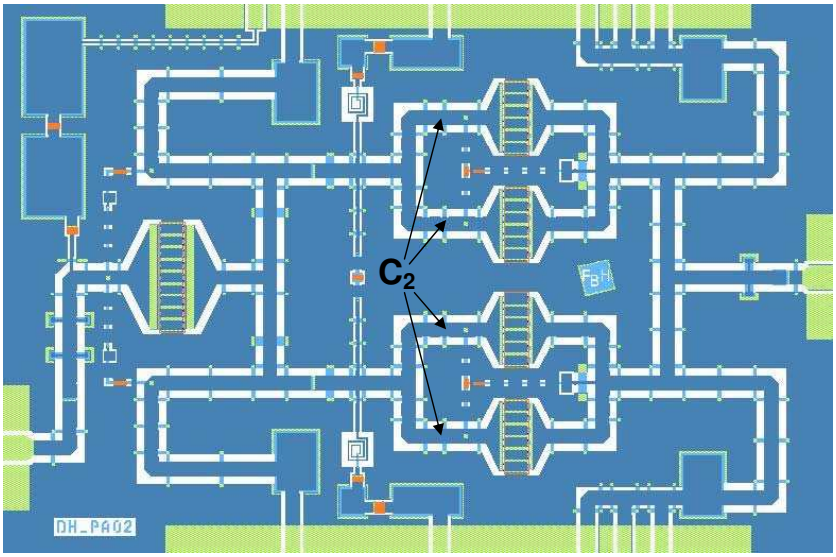

Figure 4.13: Layout of the developed power amplifier MMIC (chip size is $3{\times}4mm^2$).

Decoupling capacitor C_3 in the gate biasing network of the power stage provides nearly a short circuit at 8 GHz. Its impedance is however non-negligible in lower GHz range. The R_6-C_5 section creates an additional lossy path seen by the matching circuit in the lower GHz range. This further improves the stability at lower frequencies. Gate biasing network of the driver transistor is based on same approach.

Possible development of odd-mode oscillations within each of the two transistor pairs of the power stage was prevented by connecting the gates by R_2 resistors. Similarly, odd-mode oscillations which can exist between the transistor pairs are prevented by resistor R_3.

The maximum current that can flow through a cross section of a coplanar center-conductor limits the use of coplanar lines for high-power amplifier design. The two stubs feeding the drain current to the power stage transistors each carry a maximum current of $0.8A$, when the amplifier is driven into saturation. This current corresponds to around 70% of the maximum current flow capacity, above which electron migration starts to occur. The distance between the pads in the shown layout is compatible with the standard $150\mu m$-pitch

test probes/needles. The pads were made sufficiently large for wire-bonding. The input and the output signal pads were made sufficiently wide to accommodate two bonding wires placed in parallel, which will reduce the parasitic inductances.

4.5 Predicted Performance

Models of the passive structures for circuit simulations in ADS were provided by FBH. S-parameter of the inductors and combiners were based on electromagnetic simulations. Analytical scalable models of the coplanar elements were available in the design kit. These encompasses MIM capacitors, coplanar lines and coplanar discontinuities such as T-junctions, 90°-bends and underpasses.

Fig.4.14 shows the simulated small-signal S-parameters for the developed PA. Simulated S_{21} drops by 1 dB at 7.7 GHz and 8.4 GHz. In this frequency range, $|S_{11}|$ and $|S_{22}|$ return losses, are better than 8 and 7 dB, respectively.

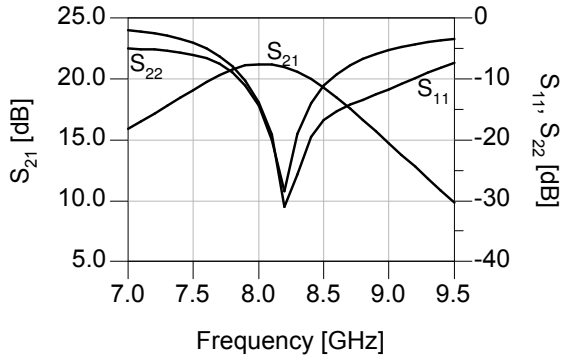

Figure 4.14: Simulated S-parameters of the power amplifier.

As indicated before, the transistor model was not capable to accurately predict the behavior of the device at high power levels. Analysis presented below estimates the achieved PAE and output power capability, based on the measured and scaled transistor data and the small-signal simulations of the amplifier circuit at 8 GHz. Impact of harmonic tuning is not considered. The estimated results are afterwards compared to the simulated ones.

In the power-sweep test, the 8-finger device biased at 80 mA/mm delivered 33.4 dBm in $1dB$ compression. The scaled 12-finger power-stage device is expected to produce 1.8 dB higher power as mentioned in the section 4.2. Four of such devices together deliver 6 dB more power. Total power delivered to the output matching circuit becomes

$$P_{o2} = 33.4 + 1.8 + 6 = 41.2[dBm] \tag{4.8}$$

Simulated power loss in the output matching circuit is 0.8 dB. The predicted power delivered by the amplifier to the 50Ω load becomes

$$P_{OUT} = P_{o2} - 0.8 = 40.4[dBm] = 11[W]. \tag{4.9}$$

Calculated in same manner, saturated output power becomes $42.5dB$.

Simulated power gain of the interstage matching circuit was $-2.5dB$. Measured input power for the 8-finger HEMT was $21dBm$ in $1dB$ compression. Power delivered by the driver transistor can now be estimated by applying the scaling rules as in the eq.(4.8),

$$P_{o1} = 21 + 1.8 + 6 + 2.5 = 31.3[dBm]. \tag{4.10}$$

Based on the the estimated output powers and periphery ratio 1/2.7, the difference between the output power densities of the two respective stages can also be found,

$$P_{o2} - P_{o1} + 10\log_{10}(1/2.7) = 41.2 - 31.3 - 4.3 = 5.6[dBm]. \tag{4.11}$$

The calculated power density ratio indicate that the driver operates at 5.6 dB lower power density as compared to the power stage, when the later is in $1dB$ compression. Hence the driver is in $5.6dB$ back-off.

At the power levels P_{o1} and P_{o2} the two respective stages draw 232 mA and 1.1 A, respectively, according to the measured device data.

Total amplifier power gain under $1dB$ compression is found from the simulated small-signal $S_{21}[dB]$

$$G = 10\log_{10}\left[\left(10^{S_{21}[dB]/20}\right)^2\right] - 1dB = 20dB = 100. \tag{4.12}$$

The power added efficiency of the whole amplifier can finally be calculated as

$$PAE = P_{OUT}\frac{1-1/G}{P_{dc1}+P_{dc2}} \tag{4.13}$$

$$= 11.1W\frac{1-1/100}{28V(0.232A+1.1A)} = 29.2\% \tag{4.14}$$

where P_{dc1} and P_{dc2} are the powers delivered by the $28V$ supply to the driver and power stage, respectively. Apparently, the estimated PAE is significantly lower as compared to the PAE of the single transistor, 39.6%, measured in $1dB$ compression. The degradation mainly comes from output combiner loss and P_{dc1}, while the total amplifier gain G is only responsible for 0.5% of the degradation.

As already pointed out, if the number of the driver device fingers is reduced from 18 to 12, and same power loss is assumed in the interstage matching circuit, the driver would exhibit unchanged output power but higher power density and consequently higher efficiency. According to the power measurement data, the DC-current flowing into the driver stage would be expected to decrease to 180 mA, so the predicted two-stage PAE would have increased to 30.4%. The disadvantage of the smaller driver periphery would be reduction of the driver back-off from $5.6dB$ to $3.9dB$.

Power added efficiency of the power stage transistors peaks in $2.5dB$ compression according to the measurements. When the calculation presented in the eq.(4.8-4.14) was repeated at this power level, PAE and driver back-off became 31.3% and $2.7dB$, respectively. The predicted PA performance is summarized in the Table 4.2.

	$1dB$ compression	$2.5dB$ compression	saturation
P_{OUT}	$40.4dBm$	$41.4dBm$	$42.5dBm$
PAE	29.2%	31.3%	
driver back-off	$5.6dB$	$2.7dB$	

Table 4.2: Estimated large-signal performance of the GaN HEMT power amplifier.

As already mentioned, large-signal model of the power HEMT overestimates the measurements with respect to the output power. This overestimation consequently occurs in connection with the entire PA. The large-signal simulations of the PA are presented in Fig. 4.15.

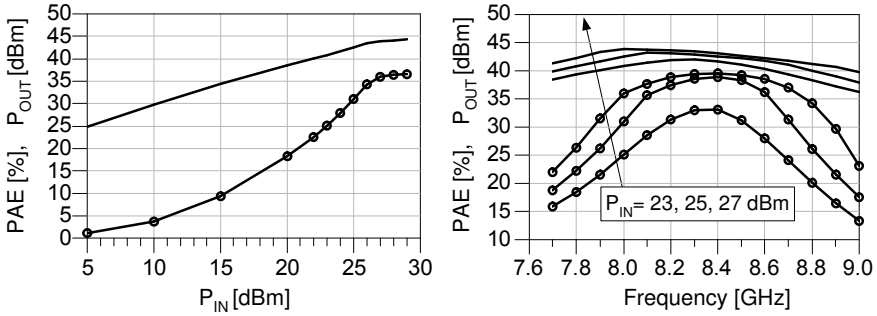

Figure 4.15: Simulated output power (-) and PAE (-o-) of the PA at 8 GHz (left plot) and with input power as parameter (right plot). At P_{IN}=27dBm the PA is driven into 3dB compression at 8 GHz.

From the left plot in the Fig. 4.15 it can be concluded that maximum P_{OUT} and peak PAE are respectively 44.3 dBm and 36%. Both of these significantly exceed the predicted data from the Table 4.2. Variation of P_{OUT} within 7.9-8.4GHz band for satellite uplink is 1.5-2.5 dB for the three shown curves in the right plot.

4.6 Discussion

One-tone measurements of the power HEMT suggested deep class-AB (80 mA/mm) as a very favorable option with respect to gain and power added efficiency. Two-tone measurements were unfortunately only possible at frequencies as high as 2 GHz. According to these measurements the deep class-AB bias also offered lowest IMD3 distortion at power levels beyond 1dB back-off. The IMD3 was better than -30 dBc at the power levels up to around 2dB compression. The two stages of the developed PA MMIC were biased at that current density. The circuit is being fabricated.

Simulated 2$^{\text{nd}}$ harmonic impedances, needed for efficiency maximization, result in voltage and current waveforms that remind those

of a parallel-tuned amplifier with shorted harmonics. Realized output and interstage matching circuits nearly approximate the optimal harmonic impedances required by the power stage transistors. In $2dB$ back-off, the obtained PAE was about 2% below the optimum case. The most undesirable harmonic terminations were those that created open circuits seen by the intrinsic device input and output.

Investigation of the transistor model also revealed that feedback capacitance C_{GD}, beside C_{DS}, significantly reduces the optimal load impedance at the fundamental frequency.

The obtained small-signal insertion gain is $21dB$, and it falls by $1dB$ at 7.7 and 8.4 GHz. Hence $1dB$ gain variation is obtained in the satellite uplink band 7.9-8.4 GHz. Without accounting for possible improvement coming from the harmonic manipulation, peak PAE of 31.3% and 42.5 dBm (18 W) saturated output power can be expected based upon device measurements and simulated circuit losses. These results are competitive to the other GaN HEMT two-stage state-of-the-art MMIC results presented in the Fig3.1 [32, 33, 35, 36].

Chapter 5

SiGe and InP based HBTs

As stated in the chapter 3 in connection with the technology investigation, millimeter-wave SiGe HBT and InP HBT technologies offer attractively high power densities. The section 3.4 outlined basic properties of the InP HBT technology from Alcatel-Thales III-V Lab and SiGe HBT technology from IHP. Excellent transport properties of InP compound and relatively high breakdown field makes the InP HBTs suitable for mm-wave power applications. For instance, mobility higher than that in Si, relaxes the trade-off between the base resistance and f_t, which both are dependent on base doping level [53]. Despite of these advantages, InP HBT based MMICs operating in 68-85 GHz range, demonstrated lower output powers (up to 80 mW) than their SiGe counterparts (up to 125 mW), as depicted in the Fig.3.3. Aggressive scaling of SiGe HBTs reduces the parasitics thereby improving the achievable gain demanded by the mm-wave amplifiers. Another advantage of the SiGe HBT technology lies in a thermal conductivity of Si, which is around twice that of InP substrate.

Goal of this chapter is to compare the two types of HBTs in terms of model parameters and a simulated performance. An accurate model of the ATL's InP HBT was available as discussed in chapter 3. In this work IHP's SiGe HBT was characterized using a large-signal compact model VBIC. First part of this chapter deals with the extraction of the model parameters from electrical measurements, and model verification. The modeling part includes the description of the developed method for accurate de-embedding of the test structure parasitics from

the small-signal measurements. After that, advantages and limitations of the SiGe and InP HBTs will be presented, together with the preliminary considerations for the InP HBT power amplifier design.

5.1 Modeling of SiGe HBT

Evaluation of power performance of the $0.21 \times 0.84\mu m^2$ HBT requires an accurate large-signal model. One commercial physics-based model of a bipolar transistor is a vertical bipolar inter-company model (VBIC) [173]. SiGe HBTs exhibiting f_t of $60GHz$ [174] and $75GHz$ [175] have been accurately characterized using the VBIC, when measured up to $26.5GHz$ and $50GHz$, respectively.

Development of a small-signal equivalent model based on a multibias S-parameters of a SiGe HBT is an essential step towards the extraction of VBIC model parameters [174, 176]. Prior to this step, parasitic effects of the RF probe pads and interconnects must be removed from the measured S-parameters. A widely used de-embedding method developed by Cho and Burk [177] employs four standard test structures - two shorts, open and thru - for characterization of the parasitics surrounding the device. Few standards provide limited information about the parasitics. This method therefore assumes that the pad and the associated interconnecting line are each representable by a single one-port impedance box. However, as the operation frequency increases, this simplified model may cease to be accurate because of distributed nature of the interconnects. More advanced methods account for the line distribution in different ways: by separate measurement of an on-wafer interconnect assisted by EM-simulation [139], by fitting all lumped-element model parameters to the structure measurements [178], or by measuring a number of additional standard structures [179].

In this work, a simplified variant of the Cho-Burk de-embedding method [180] based on only two standard structures, open and short, was further developed to account for the distribution of the interconnect admittance. The distribution of the line admittance was estimated by optimization of one empirical factor. Hereafter, the de-embedded measurement results are applied for a direct parameter ex-

traction of the small-signal equivalent circuit parameters following the procedures previously reported in [174] and [181]. Additionally, a de-embedding error resulting from probe positioning inaccuracy will be identified and corrected. The small-signal model is utilized for parameter extraction for the large-signal VBIC model based on small-signal and DC measurements. Finally, the VBIC model is experimentally verified against measurements up to 50 GHz.

5.1.1 De-Embedding of the Test Structure Parasitics

De-embedding of the RF-probe and interconnect line parasitics is prerequisite for accurate interpretation of the device characteristics. S-parameters provided by IHP were obtained from the 4-finger HBT structure illustrated in the Fig.5.1. The HBT is connected to the probe pads by finite-ground coplanar wave-guides (CPWs). The two CPW lines are to the first order of approximation described by two π-networks on each side of the device as shown in the Fig.5.2. Elements $Y_{pad(11/22)}$ and $Y_{inn(11/22)}$ model the distributed capacitive coupling of the interconnect lines and the pads to the ground. The series elements Z_{pb}, Z_{pc} and Z_e have predominately inductive behavior. Coupling between the lines due to the gap where the device is situated is modeled through Y_{bc}.

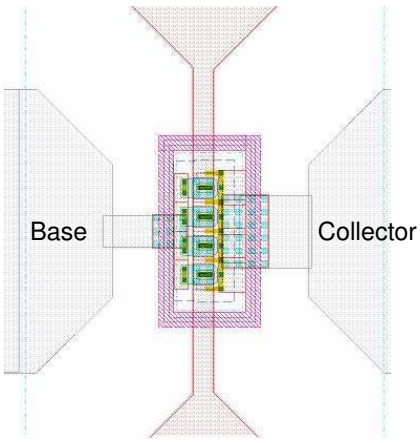

Figure 5.1: Central part of the test structure showing four parallel coupled $0.21 \times 0.84\mu m^2$ HBTs [141].

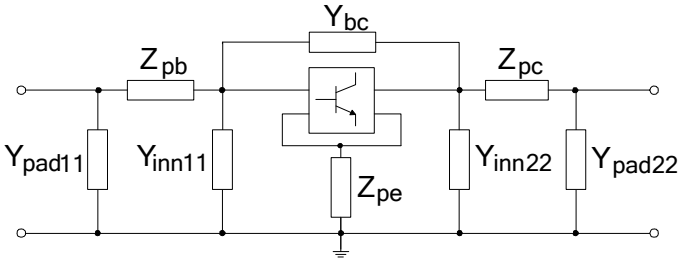

Figure 5.2: Equivalent circuit model for the HBT test structure.

Total admittances of the two interconnect lines are calculated from the open standard admittance parameters, and used for construction of the admittance matrix Y_{line}, as

$$Y_{line} = \begin{bmatrix} Y_{open11} + Y_{open21} & 0 \\ 0 & Y_{open11} + Y_{open12} \end{bmatrix}. \tag{5.1}$$

In the next step, an empirical factor n is introduced in order to divide the total line admittance, into Y_{pad} and Y_{inn} contributions as

$$Y_{pad} \simeq Y_{line} \cdot (n) \tag{5.2}$$

$$Y_{inn} \simeq Y_{line} \cdot (1 - n) \tag{5.3}$$

For $n = 1$, the total admittance would be associated with the pads, and the equivalent circuit would reduce to the conventional Cho-Burk topology [177]. For $0 < n < 1$ it would be distributed. Approximations in the equations (5.2) and (5.3) rely on the fact that the two series networks, Z_{pb}-Y_{inn11} and Z_{pc}-Y_{inn22}, respectively, resonate at much higher frequencies than the highest measurement frequency of 50 GHz.

Series impedance elements can now be extracted as

$$Z_p = [Y_{short} - Y_{pad}]^{-1} \tag{5.4}$$

$$Z_{pe} = Z_{p12} \tag{5.5}$$

$$Z_{pb} = (Z_{p11} - Z_{p21}) \cdot n_{shift} \tag{5.6}$$

$$Z_{pc} = (Z_{p22} - Z_{p12}) / n_{shift} \tag{5.7}$$

where Y_{short} is the admittance matrix of the short-standard measurement, and n_{shift} is introduced to correct a de-embedding error resulting from probe positioning inaccuracy. If the probe reference planes in the HBT structure measurements are shifted as compared to the reference planes in the short-standard measurement, a Z_{pb} and Z_{pc} impedances would be miss-predicted. A simple way to correct for this is to multiply Z_{pb} and divide Z_{pc} by a same factor n_{shift}. A procedure for estimating n_{shift} from transistor access inductances will be explained later in this section.

The inductive part of the series element Z_{pc} is plotted vs. frequency in the Fig.5.3, for two values of the distribution parameter n. For n=1, the total line admittance to the ground is concentrated in the pad, leading to a frequency dependence of the inductance L_{pc}. For n=0.5, the admittance to the ground is distributed along the line. The resulting L_{pc} becomes also less dependent on frequency. Frequency dependence of L_{pc} in the low-frequency range is believed to stem from uncertainties in the S-parameter measurements. When n=0.5 was assumed, reduced frequency dependence was correspondingly observed in the extracted small-signal equivalent circuit element values of the investigated HBT. Therefore, 0.5 was adopted as an optimum value for the de-embedding parameter n.

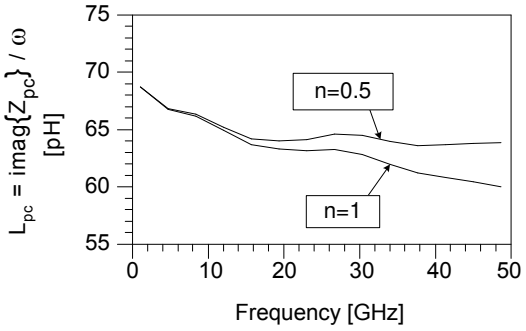

Figure 5.3: Extracted inductance of the line connecting the collector with the test probe.

The calculated two-port parameters of the equivalent circuit elements are now easily subtracted from the measured multi-bias transistor parameters in following four steps.

$$Y_{d1} = Y_{meas} - Y_{pad} \tag{5.8}$$

$$Y_{d2} = \left\{ Y_{d1}^{-1} - \begin{bmatrix} Z_{pb} & 0 \\ 0 & Z_{pc} \end{bmatrix} \right\}^{-1} \tag{5.9}$$

$$Y_{d3} = Y_{d2} - Y_{inn} - \begin{bmatrix} Y_{bc} & -Y_{bc} \\ -Y_{bc} & Y_{bc} \end{bmatrix} \tag{5.10}$$

$$Z_{d4} = Y_{d3}^{-1} - Z_{pe}. \tag{5.11}$$

Here, Y_{meas} it the measured admittance matrix of the transistor including the test structure, and Z_{d4} is the obtained Z-matrix of the transistor alone.

5.1.2 Extraction of the Small-Signal Equivalent Circuit Parameters

The carefully de-embedded small-signal parameters of the HBT are in following applied for direct parameter extraction for the small-signal equivalent HBT circuit. The applied extraction method relies on small-signal S-parameters measured under different bias conditions in cut-off, forward active and saturation mode of operation. The small-signal equivalent circuit useful to represent a SiGe HBT biased in a forward active mode was presented in [182] and is reproduced in Fig.5.4.

The bias-dependent intrinsic part of the circuit from the Fig.5.4 describes the active device in the vertical structure under the emitter. The hybrid-π topology is compatible with the large-signal model of the intrinsic transistor in VBIC model. Frequency dependence of the transconductance g_m is controlled by the parameter τ. It accounts for the excess-phase shift, which becomes noticeable as the frequency approaches f_t. The C_{bc} is the depletion capacitance while C_{be} contains both depletion and diffusion components. The intrinsic base resistance R_b is modulated by the mobile carrier concentration in the neutral base, and by the base width variation due to Early effect.

The extrinsic part of the equivalent circuit from the Fig.5.4 includes the external passive parasitics as well as the parasitic pnp tran-

sistor, existing between the substrate, base and collector of the HBT. The fixed resistors R_{bx}, R_e and R_{cx} account for access resistances between the device terminals and the intrinsic device including the contact resistances. In modern SiGe HBTs significant contribution to the device capacitances originates from the oxide capacitances. These are represented by C_{beo} and C_{bco}. Action of the parasitic pnp device biased in cut-off is accounted through the C_{bcx}, R_s and C_{cs} elements.

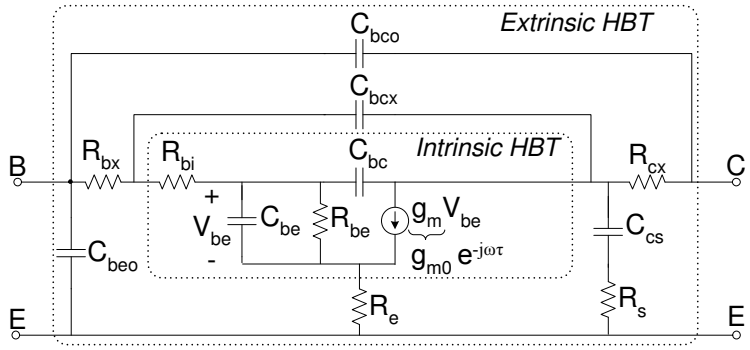

Figure 5.4: Small-signal equivalent circuit of a SiGe HBT biased in forward active mode.

Fixed Oxide Capacitances

Base-collector and base-emitter oxide capacitances were extracted from cut-off mode measurements at lower frequencies, where g_{m0} approaches zero and the access resistors and R_{be} can be neglected. Sum of total B-E and B-C capacitances were estimated from the de-embedded Y-parameters as, respectively,

$$C_{in} = \Im\left(Y_{11} + Y_{12}\right)/\omega \qquad \texttt{and} \qquad C_{fb} = \Im\left(-Y_{12}\right)/\omega. \tag{5.12}$$

In reverse and slightly forward biased regime, each of the two calculated total capacitances can be represented as a sum of a constant oxide capacitance and a bias-dependent depletion capacitance i.e.,

$$C_{in} = C_{beo} + \overbrace{\frac{C_{je}}{\left(1 - \frac{V_{be}}{P_e}\right)^{M_e}}}^{C_{be}}, \quad C_{fb} = C_{bco} + \overbrace{\frac{C_{jc} + C_{jep}}{\left(1 - \frac{V_{bc}}{P_e}\right)^{M_c}}}^{C_{bc}+C_{bcx}}. \qquad (5.13)$$

Here, V_{be} and V_{bc} are the applied bias voltages, C_{je} and C_{jc} are zero-bias depletion capacitances, P_e and P_c are built-in potentials and M_e and M_c are grading terms of the two respective junctions. C_{jep} is the extrinsic base-collector zero-bias depletion capacitance.

The parameters of the total B-C capacitance were extracted by fitting $(C_{fb} - C_{bco})$ vs. $(1 - V_{bc}/P_e)$ function to a straight line in a double-logarithmic plot [174], as shown in Fig.5.5. For an arbitrary value of C_{bco} the other parameters of the depletion capacitance equation were numerically optimized to fit $(C_{fb} - C_{bco})$. This function closely resembled a straight line when a value of $8.2fF$ was chosen for C_{bco}. Parameters of the total base-emitter capacitance were extracted in the same manner. The extracted values are summarized in the Table 5.1.

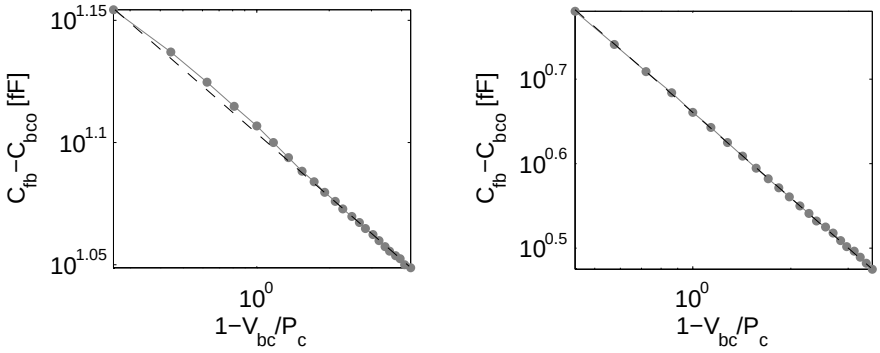

Figure 5.5: Extraction of C_{bco} at V_{ce}=$0V$, based on the shape of $(C_{fb} - C_{bco})$ vs. $(1 - V_{bc}/P_c)$ curve. Left: $C_{bco} = 0$. Right: $C_{bco} = 8.2fF$.

Fixed Access Resistances

An HBT biased in a deep saturation mode can be represented by a simple T-network of three resistors corresponding to the extrinsic

Parameter	C_{bco}	$C_{jc} + C_{jep}$	P_c	M_c
Value	8.2 fF	4.9 fF	0.724 V	0.363
Parameter	C_{beo}	C_{je}	P_e	M_e
Value	2 fF	10.2 fF	0.9 V	0.232

Table 5.1: Extracted oxide capacitances and parameters for base-emitter and base-collector depletion capacitances.

elements R_{bx}, R_{cx}, and R_e and the associated series inductors [183]. The reason is that both transistor junctions are forward biased, so the dynamic junction resistances short the junction capacitances. Small-signal measurements were provided at high base currents ranging from 0.6 to 6 mA. The current flowing into the base was equally distributed between the current flowing out of the collector and the emitter. After de-embedding the oxide capacitances the fixed resistances were found by taking the real part of the Z-parameter equations [183]

$$Z_{11} - Z_{12} = R_{bx} + j\omega L_{bx} \tag{5.14}$$

$$Z_{12} = R_e + j\omega L_e \tag{5.15}$$

$$Z_{22} - Z_{12} = R_{cx} + j\omega L_{cx}. \tag{5.16}$$

The three resistances calculated at the highest current of 6 mA became nearly independent on frequency, as depicted in Fig.5.6 (left plot). The fixed resistors were found by extrapolating the extracted values to infinite base-current limit, as depicted in Fig.5.6 (right plot). The extrapolated resistance values are summarized in Table 5.2.

Parameter	R_{bx}	R_B	R_{cx}
Value	7.5 Ω	9 Ω	2.8 Ω

Table 5.2: Extracted access resistances of the $4{\times}0.21{\times}0.84\mu m^2$ HBT.

The inductive contribution of the leads between the intrinsic transistor and the external contacts can be extracted by taking imaginary part of the eq.(5.14-5.16). Negative collector inductance and relatively large base inductance were derived using this procedure. Adding $3pH$ to the L_{cx} and subtracting the same from the L_{bx} would balance both inductances. This indicated that the probes in the HBT measurement

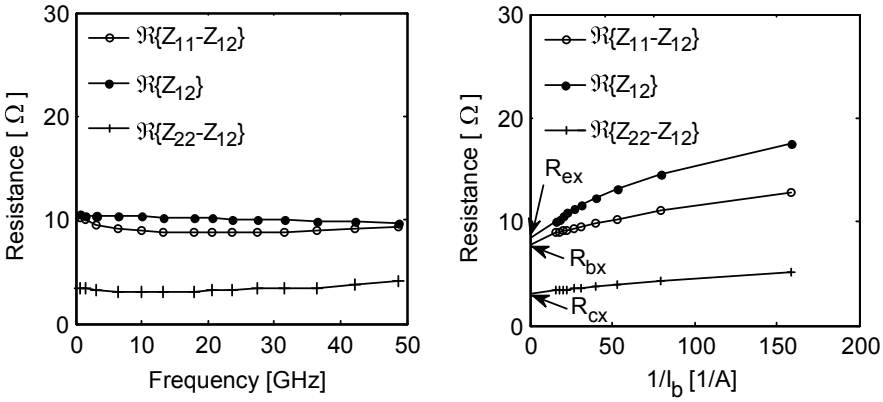

Figure 5.6: Extraction of access resistances. Left: Extracted values of Z-parameter equations at I_b=6mA. Right: Extrapolation of the averaged Z-parameters to I_b=∞.

setup could have been shifted around 3μm towards the collector side compared to the probe location in the short-standard measurements. The error was compensated by introducing the factor n_{shift}=1.05 in eq.(5.6) and eq.(5.7) in the de-embedding procedure, since the 3pH inductance corresponds to ∼5% of the inductance of the interconnects Z_{pb} and Z_{pc} in the equivalent circuit of the test structure. After the compensation, the two access inductances became negligibly small, 0.9pH, and were therefore omitted from the equivalent HBT circuit.

Substrate Parasitics

Parasitic coupling to the substrate is modeled through the series connected substrate resistance R_s and collector-substrate junction capacitance C_{cs} elements in the Fig.5.4. Provided Y-parameters were obtained from the HBT biased in cut-off. Collector-substrate voltage was swept from reverse to a weak forward polarization. Extraction of the substrate parasitics is possible after the fixed capacitances and base and collector resistances have been removed. Neglecting the emitter resistance, the two substrate parasitic elements were estimated from the Y-parameters in the low frequency range as proposed in [182],

$$R_s \simeq \Re\left(\frac{1}{Y_{11}+Y_{12}}\right), \qquad C_{cs} \simeq -\left\{\Im\left(\frac{1}{Y_{11}+Y_{12}}\right)\right\}^{-1}. \quad (5.17)$$

The extracted C_{cs} was afterwards fitted to the usual depletion capacitance expression, as those in eq.(5.13), omitting the oxide capacitance term and using the corresponding VBIC parameters, M_s, P_s and C_{jcp}. The extracted values are listed in the Table 5.3.

Parameter	R_s	M_s	P_s	C_{jcp}
Value	800 Ω	0.14	0.72 V	3.1 fF

Table 5.3: Extracted parameters of the parasitic substrate network.

Hybrid-π Equivalent Circuit

Reverse biased base-emitter junction of the parasitic pnp device contributes to the base-collector capacitance through C_{bcx} element in the equivalent circuit of the Fig.5.4. The elements of the intrinsic device together with C_{bcx} can be calculated after stepwise de-embedding of the previously calculated elements in following order: oxide capacitances, access resistances in base and collector, substrate-collector parasitics and finally emitter resistance. The method applied in [180] was used here to extract the remaining elements of the equivalent circuit. The influence of C_{bcx} is first removed by manipulating the de-embedded Y-parameters as

$$Y_a = Y_{11} + Y_{12} = \frac{g_{be} + j\omega C_{be}}{1 + R_{bi}\left(g_{be} + j\omega\left(C_{be} + C_{bc}\right)\right)} \quad (5.18)$$

$$Y_b = Y_{21} - Y_{12} = \frac{g_{mo}e^{-j\omega\tau}}{1 + R_{bi}\left(g_{be} + j\omega\left(C_{be} + C_{bc}\right)\right)} \quad (5.19)$$

$$Y_c = Y_{22} + Y_{12} = \frac{j\omega C_{bc}R_{bi}\left(g_{be} + g_{mo}e^{-j\omega\tau} + j\omega C_{be}\right)}{1 + R_{bi}\left(g_{be} + j\omega\left(C_{be} + C_{bc}\right)\right)} \quad (5.20)$$

where $g_{be} = 1/R_{be}$ is introduced. Using the calculated Y_a, Y_b and Y_c, following useful subfunctions are defined,

$$a = \frac{1}{|Y_b|_{\omega\to 0}} = \frac{1 + R_{bi} g_{be}}{g_{mo}}, \tag{5.21}$$

$$b = \frac{1}{\omega}\sqrt{\frac{1}{|Y_b|^2} - a^2} = \frac{R_{bi}\left(C_{be} + C_{bc}\right)}{g_{mo}}, \tag{5.22}$$

$$c = \Re\left(\frac{Y_a}{Y_b} e^{-j\omega\tau}\right) = \frac{g_{be}}{g_{mo}}, \tag{5.23}$$

$$d = \Im\left(\frac{Y_a}{Y_b} e^{-j\omega\tau}\right)\frac{1}{\omega} = \frac{C_{be}}{g_{mo}}, \tag{5.24}$$

$$\tau_{RC} = \Im\left(\frac{Y_c}{\omega\left(Y_a + Y_b\right)}\right) = R_{bi} C_{bc}, \tag{5.25}$$

where the excess phase delay parameter τ is found from

$$\omega\tau = -\left(\angle Y_b + \arctan\left(\omega b/a\right)\right) \tag{5.26}$$

Remaining circuit elements are extracted by solving the eq.(5.21-5.25) as follows

$$R_{bi} = \frac{b - a\tau_{RC}}{d - c\tau_{RC}}, \tag{5.27}$$

$$g_{mo} = \frac{1}{a - cR_{bi}}, \tag{5.28}$$

$$R_{be} = c g_{mo}, \tag{5.29}$$

$$C_{be} = d g_{mo}, \tag{5.30}$$

$$C_{bc} = \frac{\tau_{RC}}{R_{bi}}, \tag{5.31}$$

$$C_{bcx} = \Im\left(-Y_{12} - \frac{j\omega C_{bc}}{1 + R_{bi}\left(g_{be} + j\omega\left(C_{be} + C_{bc}\right)\right)}\right)\frac{1}{\omega} \tag{5.32}$$

Some of the calculated element values are plotted vs. frequency in the Fig.5.7. In general, reasonably low frequency dependence is obtained in a wide range of the operating conditions. Above $\sim$18 GHz, $\omega\tau$ grows almost linearly with frequency, as expected. Extracted element values of the hybrid-π equivalent network are summarized in the Table 5.4. It can be seen from the table that the C_{bc} value is slightly

higher at V_{ce}=1.5V as compared to the value at 1.0V. This trend is inconsistent with the expected voltage dependence of a depletion capacitance - C_{bc} should decrease with increasing V_{ce}. However, the sum (C_{bc}+C_{bcx}) does decrease with V_{ce}. In fact, it has been found that the model response is mainly affected by the sum (C_{bc}+C_{bcx}), while the accurate distribution between the intrinsic and extrinsic capacitance is of less importance.

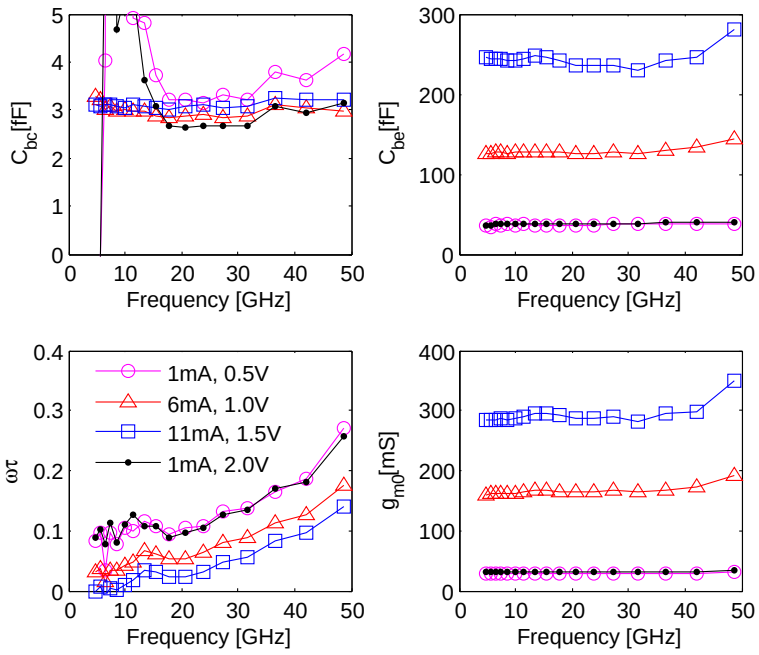

Figure 5.7: Frequency dependence of the extracted element values for the intrinsic device.

I_c/V_{ce}	R_{bi} [Ω]	C_{bc} [fF]	C_{be} [fF]	R_{be} [Ω]	g_{mo} [mS]	τ [pS]	C_{bcx} [fF]
$1mA/0.5V$	50	3.4	37	2743	29	0.81	2.1
$6mA/1.0V$	60	2.9	127	578	165	0.47	1.5
$11mA/1.5V$	60	3.1	240	280	290	0.26	0.95
$1mA/2.0V$	53	2.8	38	2992	31	0.79	0.16

Table 5.4: Extracted element values for the hybrid-π equivalent circuit of the $4 \times 0.21 \times 0.84\mu m^2$ SiGe HBT at four bias points.

Verification of the Small-Signal Equivalent Model

In order to verify the de-embedding and the extraction procedure, simulated S-parameters of the equivalent circuit, are compared to the measured and de-embedded S-parameters as shown in Fig.5.8. Excellent agreement is achieved up to the highest measurement frequency of $50GHz$. The small-signal equivalent circuit is capable of predicting the behavior of the HBT beyond the maximum-f_t current of $\sim 8mA$. The accuracy of the model would cease if the extraction is attempted in quasi-saturation region, where the B-C junction is forward biased.

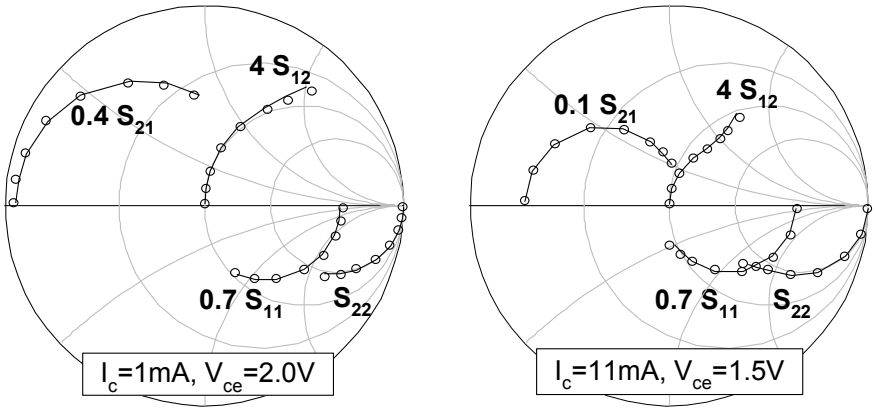

Figure 5.8: Measured (o) and modeled (-) S-parameters in frequency range 0-50 GHz at two bias conditions.

5.1.3 Parameter Extraction for VBIC95 Model

Large-signal modeling of the SiGe HBT was carried out in order to evaluate the large-signal performance of the device at E-band. For this purpose, a VBIC95 model [173] is used. The VBIC95 model covers several important effects in the bipolar devices: Early effect, quasi-saturation, collector resistance modulation, avalanche multiplication and self-heating. Equivalent network of VBIC95, shown in Fig.5.9, includes an intrinsic npn transistor, a parasitic substrate pnp transistor, parasitic resistances and capacitances, a thermal network, and a network that implements excess phase for the forward transport current.

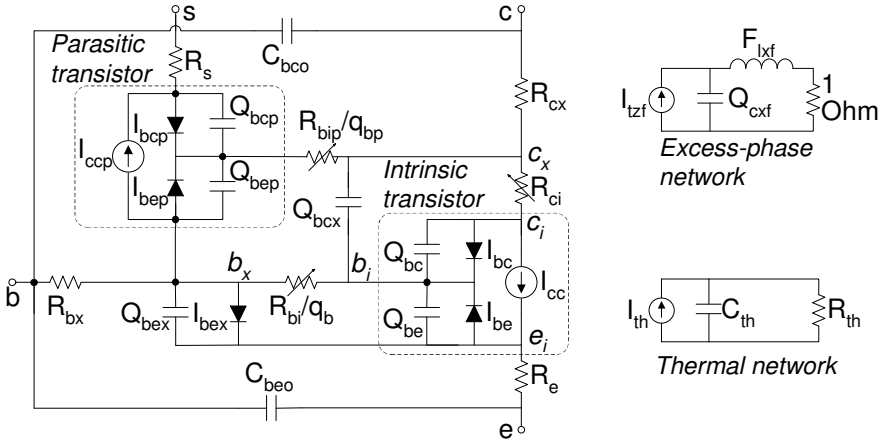

Figure 5.9: VBIC95 model equivalent network

Modeling of avalanche multiplication and self-heating was not carried out in this work. The parameter extraction described below is based on pre-knowledge of the thermal resistance $R_{th} = 2200\Omega$, and weak avalanche parameters $AVC_1 = 2$ and $AVC_2 = 11.1$. These parameters were provided in an outdated set of VBIC parameters of IHP's 4-finger SiGe HBT having same emitter dimensions.

Some of the extracted values of the small-signal equivalent circuit elements, like fixed capacitances and resistances and parasitic substrate resistance, were directly used as parameters for the large-signal VBIC95 model. Parameters for the depletion capacitances were used as well. The total C-B zero-bias depletion capacitance of 4.9 fF, presented in Table 5.1, was partitioned into the intrinsic C_{jc} and extrinsic C_{jep} component using the C_{bc}/C_{bcx} ratio of 2.5 extracted at peak f_t.

Excess-phase parameter τ presented in Table 5.4 ranges between $0.8pS$ at $1mA$ and $0.26ps$ at $11mA$. Since the excess phase delay in the VBIC model is independent on the bias, an average value of 0.4 ps was used for the excess phase delay parameter T_d. Such a low value of the excess phase delay is of minor importance for the small-signal S-parameters well below the cut-off frequency f_t.

Early-Effect Modeling

Modulation of the neutral base width caused by the bias dependent width of the depletion regions is called Early-effect. In a common-emitter stage this results in a finite output conductance g_o. Forward and reverse Early-voltage parameters V_{ef} and V_{er} are calculated by solving two coupled equations [173],

$$(q_{bc}^f - I_c c_{bc}^f / g_o^f)(1/V_{ef}) + q_{be}^f (1/V_{er}) = -1 \tag{5.33}$$

$$(q_{be}^r - I_e c_{be}^r / g_o^r)(1/V_{er}) + q_{bc}^r (1/V_{ef}) = -1 \tag{5.34}$$

where superscripts f and r denote forward and reverse mode of operation, respectively, q is the normalized depletion charges and c is the depletion capacitance normalized to the corresponding zero-bias depletion capacitance. Junction charge q can be calculated as follows

$$c = \frac{\delta q}{\delta V} = \frac{1}{\left(1 - \frac{V}{P}\right)^M} \Longrightarrow \tag{5.35}$$

$$q = \frac{-P}{M-1}\left(1 - \left(1 - \frac{V}{P}\right)^{(1-M)}\right) \tag{5.36}$$

where P is the built-in potential, M is the grading coefficient and V is the applied voltage for the particular junction. Calculated Early voltages for the SiGe HBT became $\underline{V_{ef} = 83V}$ and $\underline{V_{er} = 2.1V}$.

Diodes and Transport-Current Parameters

Transport current source of the intrinsic device in VBIC is given by [173]

$$I_{cc} = \frac{I_s}{q_b}\left(\exp\left(\frac{V_{bei}}{N_f V_t}\right) - \exp\left(\frac{V_{bci}}{N_f V_t}\right)\right), \tag{5.37}$$

where V_{bei} and V_{bci} are the B-E the B-C voltages, respectively, V_t is the thermal voltage, N_f and N_r are the forward and the reverse ideality factors, respectively, I_s is the saturation current and q_b is the normalized base charge. High injection in the base and Early effect are treated by modulation of q_b. The high injection effect is modeled through forward and reverse knee current parameters, I_{kf} and I_{kr},

respectively. They acts as a limitation of the exponential current increase. After the Early voltages were calculated, the transport current parameters were extracted in following steps:

- Parameters I_s and N_f were extracted from forward Gummel measurements up to moderate current level where high-injection and resistive effects are negligible. V_{bc} was set to $0V$ while V_{be} was swept in a range 0.4-0.8 V. Measured I_c versus V_{be}, plotted in the logarithmic current plot is almost a straight line, which slope is proportional to N_f, and which offset on the logarithmic scala is controlled by I_s.

- N_r was extracted from the emitter current in the reverse Gummel measurements, in which V_{bc} was swept, and V_{ce} was kept constant at -0.5 and -1.5V.

- I_{kf} and I_{kr} were optimized to fit the collector- and emitter currents to the high-current subrange of the forward and reverse Gummel measurement, respectively.

Current of the forward biased base-emitter diode is split into sum of an ideal and a non-ideal component,

$$I_{be} = I_{bei}\left(\exp\left(\frac{V_{bei}}{N_{ei}V_t}\right) - 1\right) + I_{ben}\left(\exp\left(\frac{V_{bei}}{N_{en}V_t}\right) - 1\right). \quad (5.38)$$

The ideal and non-ideal diode parameters, I_{bei}, N_{ei} and I_{ben}, N_{en}, respectively, can be extracted from the base current in the forward Gummel plot. The non-ideal parameters can be extracted in the low current range, while the ideal parameters can be extracted from the medium current range where the series resistances of the base and emitter can be neglected. The non-ideal base current turned out to be negligible all way down to 10 pA, which is an indication of a negligible recombination currents in the E-B space-charge region [184].

Current through the base-collector diode

$$I_{bc} = I_{bci}\left(\exp\left(\frac{V_{bci}}{N_{ci}V_t}\right) - 1\right) + I_{bcn}\left(\exp\left(\frac{V_{bci}}{N_{cn}V_t}\right) - 1\right). \quad (5.39)$$

is also controlled by the ideal, and non-ideal parameters, I_{bci}, N_{ci}, and I_{bcn}, N_{cn}, respectively. From measured reverse Gummel plot it is not possible to distinguish between this current and the current flowing through the B-E diode of the parasitic substrate transistor. Both diodes are characterized by the same ideality factors in VBIC, but the parasitic B-E diode has its own saturation currents I_{beip} and I_{benp}. The ideal and non-ideal saturation currents extracted from the reverse Gummel plot were partitioned into B-C and parasitic B-E saturation currents using the C_{bc}/C_{bcx} ratio of 2.5 extracted at peak f_t.

Transport current for the parasitic substrate transistor is given by

$$I_{ccp} = \frac{I_{sp}}{q_{bp}} \left(\exp\left(\frac{V_{bep}}{N_{fp}V_t}\right) - \exp\left(\frac{V_{bcp}}{N_{fp}V_t}\right) \right) \tag{5.40}$$

where V_{bep} and V_{bcp} are voltages across the parasitic B-E and the parasitic B-C diode, respectively. Saturation current I_{sp} and ideality factor N_{fp} were extracted from the substrate current in forward Gummel plot of the parasitic transistor up to moderate current level, similarly to the intrinsic npn transistor. In this measurement, emitter was floating, while the substrate-collector voltage was swept keeping V_{be} at 0.5 V. Normalized parasitic base charge q_{bp} is controlled by the knee current parameter I_{kp}, which was extracted from the substrate current in the high current region.

The base-collector current of the parasitic transistor is modeled as

$$I_{bcp} = I_{bcip} \left(\exp\left(\frac{V_{bcp}}{N_{cip}V_t}\right) - 1 \right) + I_{bcnp} \left(\exp\left(\frac{V_{bcp}}{N_{cnp}V_t}\right) - 1 \right) \tag{5.41}$$

where I_{bcip}, N_{cip} and I_{bcnp}, N_{cnp} control the ideal and non-ideal current components, respectively. The parameters were extracted from the reverse Gummel plot of the parasitic transistor, based on the same procedure as for the other diodes mentioned above. The extracted DC-parameters are listed in Table 5.5.

Quasi-Saturation Parameters

Quasi-saturation is defined as the region where the intrinsic B-C junction is forward biased, while the external B-C terminal remains reverse

Param.	*Value*	*Param.*	*Value*	*Param.*	*Value*
I_s	2e-18	N_{en}	2	N_{fp}	0.996
N_f	1.020	I_{bci}	1.65e-18	I_{kp}	0.004
N_r	1.015	I_{bcn}	3.67e-14	I_{bcip}	3.23e-15
I_{kf}	0.005	N_{ci}	1.057	I_{bcnp}	1e-25
I_{kr}	0.006	N_{cn}	2	N_{cip}	1.01
I_{bei}	6.2e-20	I_{beip}	6.62e-19	N_{cnp}	2
I_{ben}	1e-25	I_{benp}	1.47e-14		
N_{ei}	1.032	I_{sp}	2.94e-20		

Table 5.5: Extracted parameters for the diodes and transport currents.

biased [185]. In this mode of operation, minority carriers are injected into the lightly doped collector, widening the base of the device and thus reducing current gain and storing excess charge in the collector. In a device employing lightly doped collector, the quasi-saturation is more pronounced due to a high collector resistance. Moreover, collector transit-time tends to be high, reducing the f_t [186]. However, low collector doping level has a beneficial impact on break-down voltage and f_{max} due to decreased electric field and capacitance of the B-C junction, respectively [186, 187].

Parameters responsible for the device behavior in quasi-saturation are R_{ci}, γ, V_o, H_{rcf}, Q_{co}, which detailed explanation can be found in [188]. The Q_{co} is a zero-bias collector charge affecting high-frequency modeling and will be treated in the next section. The first four parameters are optimized by fitting the output characteristics in quasi-saturation and saturation region. The optimization result is shown in Fig.5.10. The extracted parameter values are presented in Table 5.6. The R_{ci} is resistance of the intrinsic collector. Increasing the R_{ci} from 18 to 30Ω in the optimization would have yielded almost perfect fit in the quasi-saturation part of the characteristic. This resistance is however almost double of what was expected from the layer properties of the device structure. This deviation of the R_{ci} from the physics based expectations will also be discussed in the next subsection in connection with transit-time modeling.

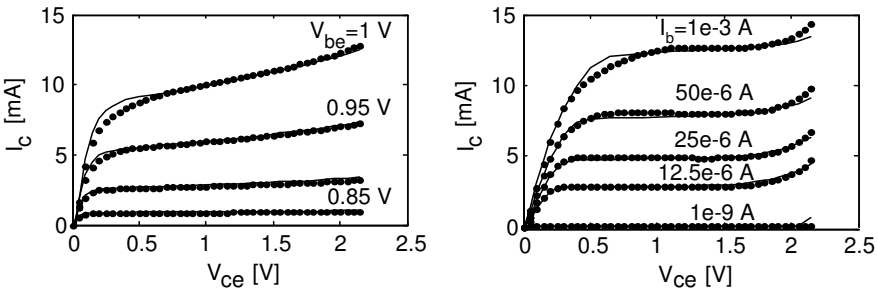

Figure 5.10: Measured (.) and modeled (-) output characteristics. Left: constant V_{be}. Right: Constant I_{be}.

Parameter	R_{ci}	γ	V_o	H_{rcf}
Value	18	1.3e-13	0.68	5.4

Table 5.6: Parameters optimized to fit the I_c-V_{ce} curves in quasi-saturation region.

AC-Parameters and Model Verification

Cut-off frequency f_t was extrapolated from the measured small-signal parameters de-embedded for the pads and interconnects as

$$f_t = h_{21} \times 10GHz \tag{5.42}$$

where h_{21} is small-signal current gain with shorted output, extracted at $10GHz$, where the slope of h_{21} was -$20dB/dec$. According to reference [189] expression for the total transit-time of an HBT is

$$\frac{1}{2\pi f_t} \simeq T_f + \frac{V_t}{I_c}\left(C_{bc} + C_{bcx} + C_{be}\right) + \left(R_{cx} + R_e\right)\left(C_{bc} + C_{bcx}\right) \tag{5.43}$$

The extracted transit time, $1/(2\pi f_t)$, is plotted vs. inverse collector current $(1/I_c)$ in Fig.5.11 (left plot). At lower currents $1/(2\pi f_t)$ increases linearly with $1/I_c$, as expected from the eq.(5.43). At infinite I_c, extrapolated transit time equals the sum of T_f, accounting for electron's transit time through the base and B-C depletion region, and the charging term accounting for parasitic series resistances, as indicated. T_f parameter is extracted from this extrapolated value.

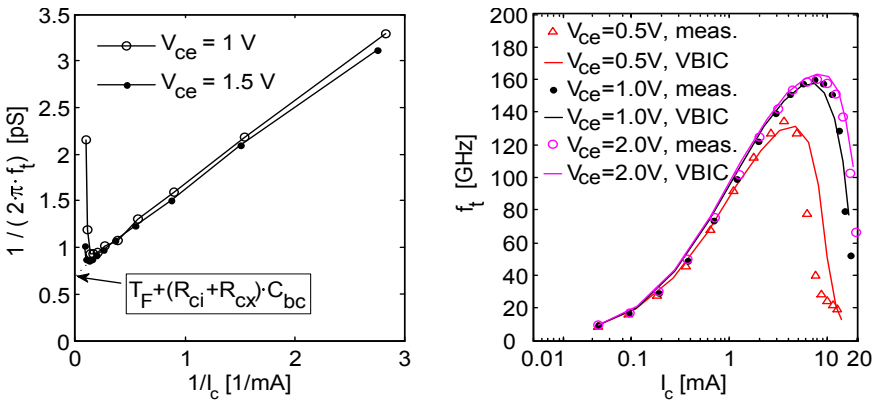

Figure 5.11: Left: Transit time extrapolated at $10GHz$ vs. inverse collector current. Right: Measured and modeled cut-off frequency f_t

The total transit time in the VBIC model is bias dependent through parameters X_{tf}, I_{tf}, V_{tf} and Q_{tf}. These parameters were optimized to fit the f_t-I_c plots in the high-current end. Results of the optimization are shown in Fig.5.11 (right plot). The quasi-saturation parameter Q_{co} was included in the optimization of the $0.5V$-curve, since at higher currents and $0.5V$ the device approaches quasi-saturation region.

As in the case of the DC output characteristics, it was not possible to accurately capture f_t in quasi-saturation using $R_{ci} = 18\ \Omega$. By increasing the R_{ci} to 30 Ω, remarkably better fit was possible. Non-physical behavior of VBIC in quasi-saturation has also been recognized by de Graaff [190]. The discrepancy between the measured and modeled DC output characteristics and f_t in quasi-saturation region will possibly lead to a slight overestimation of the output power and efficiency performance of the HBT.

Parameter R_{bi} controlling the intrinsic base resistance was optimized to fit the measured S11 and S21 parameters over a range of collector currents. The extracted AC-parameters are summarized in Table 5.7. Comparison between measured and modeled S-parameters is presented in the Fig.5.12. Good agreement was achieved up to 50 GHz, and beyond maximum-f_t current of $8mA$.

Parameter	*Value*	*Parameter*	*Value*	*Parameter*	*Value*
T_f	5.9e-12	V_{tf}	0.35	R_{bi}	145
X_{tf}	30	Q_{tf}	1e-9		
I_{tf}	0.8	Q_{co}	6e-15		

Table 5.7: Extracted VBIC AC-parameters.

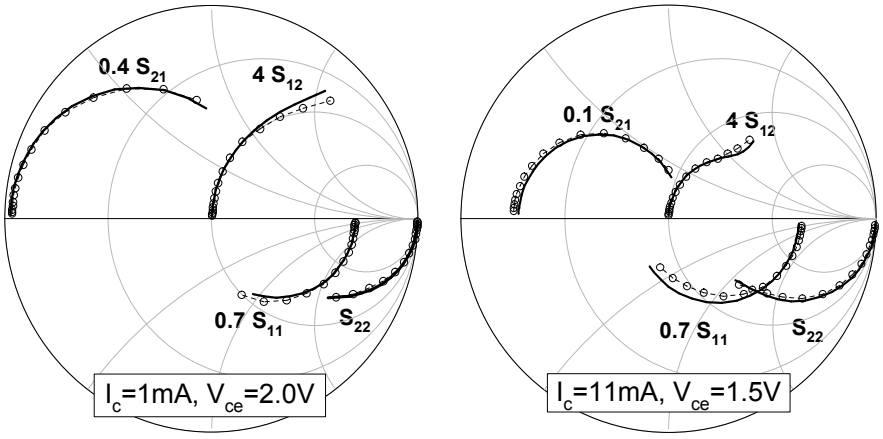

Figure 5.12: S-parameters for the $4\times(0.21\times0.84\mu m^2)$ SiGe HBT, measured (o) and simulated using VBIC (-) in frequency range 0-50 GHz at two bias conditions.

Apart from the slight discrepancy in the quasi-saturation, good consistency between measured and modeled data was achieved in 0-$50GHz$ range. Not shown are the simulated Gummel-plots as well the DC-plots of the parasitic substrate transistor, which agreed with the measured DC-data as well. In following section the VBIC model will be used to estimate the power and gain performance of the SiGe HBT at 73.5 GHz.

5.2 SiGe HBT and InP HBT Performance at E-band

The rest of this chapter will explore the possibilities of the SiGe HBT and InP HBT to act as E-band power amplifiers. The equivalent circuit parameters will provide a valuable link between the device physics

and performance. Limitations arising from the two technologies will be discussed. Preliminary considerations for the design of InP HBT power amplifier will also be presented.

5.2.1 Device Parameters

The $1.5\times10\mu m^2$ InP HBT exhibits peak in the maximum oscillation frequency f_{max} when biased at I_C=$24mA$, V_{CE}=$1.6V$. The peak f_{max} for the $4\times0.21\times0.84\mu m^2$ SiGe HBT occurs at around three times lower current and same voltage. Output power for a class-A biased device is ideally given by $0.5I_{CE}V_{CE}$. Therefore, three parallel-connected SiGe HBTs, biased at peak f_{max}, would ideally be capable to produce same power as the single InP HBT. The resulting SiGe HBT configuration could in principle be realized as a single 12-finger transistor or as two combined 6-finger units. Important parameters for the two devices are compared in the Table 5.8. The parameters for the SiGe HBT are calculated by simple $3\times$ scaling of the extracted VBIC model, neglecting the possible unwanted effects like combining losses and mutual heating between the adjacent transistors.

The superior thermal conductivity od Si as compared to InP substrate counts towards the relatively low thermal resistance R_{th} of the total SiGe HBT device as indicated in the table. Hence the SiGe device will develop lower junction temperature than InP HBT, when similar bias is applied to the devices.

It can be concluded from the Table 5.8 that InP HBT exhibits peak in f_{max} at about 7.5 times lower current density J_{bias} as compared to SiGe device. Larger zero-bias depletion capacitances C_{je} and C_{jc} of the InP HBT device offsets the advantage of lower transit time T_F, since the two devices operate at almost same I_{bias} (recall the equation 3.5). As a result, the two devices exhibit comparable f_t.

5.2.2 HBTs in Power-Amplifiers

Simulated load trajectories of the two common-emitter connected devices biased at 1.6 V and driven in $1dB$ gain compression are depicted in the Fig.5.13 (left and middle plot, respectively). The trajectories are overlayed on the constant-V_{be} output characteristics. Investigated

	SiGe HBT	*InP HBT*	Unit	Remarks
A_E	2.1	15	μm^2	Emitter area
I_{bias}	24	23	mA	
J_{bias}	11.4	1.53	$mA/\mu m^2$	
f_t	170	200	GHz	
f_{max}	170	200	GHz	
R_{th}	733	1250	K/W	
C_{je}	30.4	42	fF	
C_{jc}	14.7	32	fF	intrinsic + extrinsic
C_{beo}	6	0	fF	
C_{bco}	25	0	fF	
R_{ci}	6	6	Ω	
R_{cx}	0.9	9.4	Ω	
V_{off}	$<$0.03	0.18	V	C-E offset voltage
BV_{CEO}	1.9	$>$7	V	
T_F	0.59	0.4	ps	transit time through base and B-C depletion region

Table 5.8: Parameters of the 3× scaled ($4\times0.21\times0.84\mu m^2$) SiGe HBT and ($1.5\times10\mu m^2$) InP HBT when biased for peak f_{max} occurring at V_{CE}=1.6V. Unless stated otherwise, the parameter names have their usual meaning as defined in the VBIC model.

operating points and PA performance are summarized in Table 5.9. Optimum load impedances Z_{OPT} for maximum power output were selected based on load-pull simulations.

The SiGe HBT was biased at peak-f_{max} bias point ($1.6V/24mA$) which incidentally also is a near class-A bias point for that device. When the bias voltage was increased to $1.9V$, the output referred $1dB$-compression power P_{1dB} increased from 8.9 to 10.1 dBm, $3dB$-compression power P_{3dB} increased to $13.3dBm$. This also pushed the load cycle further beyond the break-down voltage BV_{CEO} of 1.9 V. It has been demonstrated however that the SiGe devices can tolerate such operating conditions if the bias circuit presents a low enough resistance to the transistor's base [85, 191].

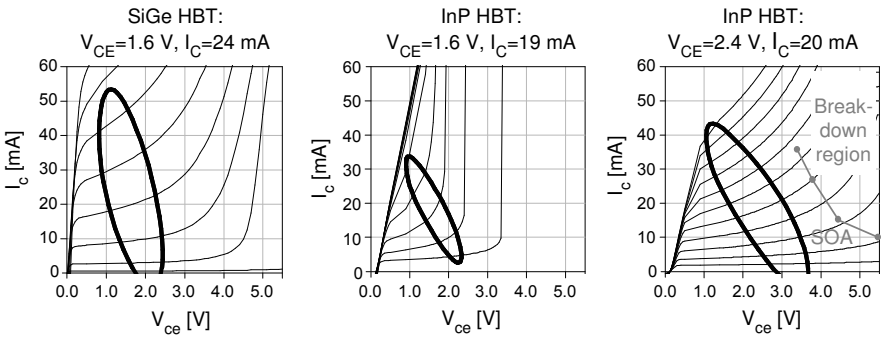

Figure 5.13: Load cycles simulated using Harmonic Balance in ADS at 73.5 GHz. Left: 3× ($4\times0.21\times0.84\mu m^2$) SiGe HBT. Middle and right: $1.5\times10\mu m^2$ InP HBT at two different operating points.

If biased for maximum f_{max}, the InP HBT would operate near saturation which would cause premature gain compression. Class-A bias is therefore provided by reducing the current from 23 to $19mA$ for that transistor as indicated in the Fig.5.13 (middle plot). As a result, the small-signal transducer gain G_t dropped from 6.75 to 6.3 dB. High collector resistance R_{cx} and C-E offset voltage V_{off} of the InP HBT presented in the Table 5.8 impedes the load trajectory to enter the low-voltage part of the output characteristics. When biased at $1.6V$, the InP HBT generated $2.5dB$ lower P_{1dB} than the SiGe HBT, as can be concluded from data in the Table 5.9.

InP HBT exhibited larger voltage swing when V_{CE} was increased to $2.4V$ as depicted in the Fig.5.13 (right plot). This resulted in superior P_{1dB} and power-added efficiency of that device. This bias point is still deep inside the safe operating area (SOA), and far below the BV_{CEO} of $7V$. The indicated break-down points provided by ATL have been obtained by imposing a constant base current [192].

In a bipolar device positive feedback exists between the current and the junction temperature [193]. This self-heating effect causes the slopes of the constant V_{be} curves in the Fig.5.13 to increase with the collector current and the collector voltage, that is, with the dissipated DC-power. The most severe effect of that mechanism is a thermal-runaway which can destroy the device. The DC characteristics in the Fig.5.13 (middle plot) indicate that safe operation of InP HBT would

	SiGe HBT	*InP HBT*		*Unit*
I_{CE}/V_{CE}	$1.6V/24mA$	$1.6V/19mA$	$2.4V/20mA$	
G_t	5.9	6.3	6.3	dB
Z_{in}	7.7-j6.1	15-j2	15-j1	Ω
Z_{OPT}	19+j22	41+j21	49+j30	Ω
P_{1dB}	8.9	6.4	11.4	dBm
P_{3dB}	12	9.4	13.4	dBm
PAE_{1dB}	13	9.6	18	%
PAE_{3dB}	18	14	23	%
T_{max}	56	64	86	$°C$

Table 5.9: Summary of performance for the three amplifiers from the Fig.5.13.

not be possible by imposing constant V_{be} at $2.4V/20mA$. Imposing a constant base current, however, would make the slope of the collector current almost independent on the dissipated power. This can be seen in the I_c-V_{ce} characteristics shown before in the Fig.3.11. Very large resistor in series with the base supply voltage would have the same effect. According to the simulations, a 320-Ω resistor would be sufficiently high. Such bias topology has been chosen for the $2.4V$ biasing. The resulting output characteristics are indicated in the Fig.5.13 (right plot). Base supply voltage was swept from 0.78 to $1.02V$ to obtain the shown curves. Operating point $2.4V/20mA$ was selected for the power amplifier development, described later in chapter 6. Eight devices can deliver total P_{1dB} of $20.4dBm$.

Device temperature under large signal excitation is calculated as

$$T = T_{amb} + R_{th}\left(P_{dc} + P_{in} - P_{out}\right) \tag{5.44}$$

where T_{amb} is the ambient temperature of 27°C, P_{dc} is the consumed DC-power, P_{in} is the generator power delivered to the device at the fundamental frequency, and P_{out} is a sum of powers delivered by the amplifier at fundamental and harmonic frequencies. Maximum temperatures T_{max} presented in the Table 5.9 were developed with no drive signal applied to the HBTs. Temperature dropped with increasing drive power. Above 2-3 dB compression level, it rose again, since

the gain (P_{out}-P_{in}) dropped rapidly. The SiGe HBT amplifier exhibited lowest temperature due to the lowest R_{th}. The $2.4V$ InP HBT developed highest temperature due to the relatively large R_{th} and P_{dc}. The temperature increase due to the thermal coupling between the three 4-finger SiGe transistors was neglected.

As argued before, high collector resistance R_{cx} is an important disadvantage of the InP HBT under investigation. To show this, the R_{cx} was reduced from 9.4Ω to a value of 0.9Ω present in the SiGe HBT. Without re-optimization of the Z_{OPT}, P_{1dB} delivered by the InP HBT ($2.4V$ bias) increased by $1.4dB$.

Another obvious difference between the SiGe HBT and InP HBT amplifier data listed in the Table 5.9 is their input impedance Z_{in} and load impedance Z_{OPT}. The impedances are much lower for the SiGe device. This would have negative impact on the bandwidth and combining losses in amplifier stages combining many devices. Large oxide capacitance $C_{bco} = 25fF$ (see Table 5.8) existing between the base and collector of the SiGe HBT significantly lowers the impedance levels of the SiGe device. With C_{bco} set to zero, as in the InP HBT, the SiGe amplifier would show substantially higher impedances, Z_{OPT}=$39.5 + j26$ and Z_{in}=$16 - j8$.

The quality factors Q (ratios between the imaginary and real parts) of the two impedances Z_{OPT} and Z_{in} also remarkably dropped when the C_{bco} was removed. A high Q of an impedance to be matched limits the achievable bandwidth as mentioned in section 4.3. It is worth to note that the gate-drain capacitance had similar effect regarding the load Q of the GaN HEMT amplifier, discussed in the section 4.3.

5.3 Discussion

This chapter explored applicability of two modern millimeter-wave HBTs for signal power generation in the middle of the E-band frequency range 71-76 GHz. For this purpose a large-signal VBIC model was utilized to characterize the 4-finger SiGe HBT from IHP foundry.

A simple technique has been suggested to account for distributed nature of transistor test structure. The method can be easily used to improve the accuracy of the conventional open-short de-embedding

techniques. A procedure for identifying and correcting a de-embedding error resulting from probe positioning inaccuracy was also suggested and applied in direct parameter extraction of the small-signal equivalent circuit elements. The subsequent extraction of the VBIC model parameters resulted in good agreement with the DC measurements and the small-signal measurements under various bias conditions, and slight discrepancy in quasi-saturation.

For operation at peak f_{max}, the SiGe HBT must draw around 7.5 times higher current per unit emitter area compared to the InP device. Three parallel connected 4-finger SiGe HBTs (or a single 12-finger device) draw same current as the single-finger InP HBT. If the temperature rise due to the thermal coupling within the three SiGe transistors was disregarded, the SiGe HBT would have developed lower temperature compared to the InP HBT, despite of much higher current density. This is primarily due to the excellent thermal management and to some extent due to relatively low bias voltage of the silicon device. Hence, the main advantage of the SiGe HBT is the good heat dissipation that enables high current density, while InP HBTs benefit from high breakdown voltage.

The SiGe transistor also showed much lower input and load impedances than the InP transistor. This is in part a consequence of high B-C oxide capacitance of the SiGe device. High breakdown voltage of the InP HBT opens the possibility to obtain higher power and efficiency and to further enhance the load impedance, compared to the 12-finger SiGe transistor. This advantage, concerning the power and efficiency, is severely diminished by high resistance appearing in the collector of the InP transistor.

Eight InP HBTs having total emitter area $8\times(1.5\times10\mu m^2)$ are capable of generating more than 100 mW E-band power under $1dB$ compression, while drawing 160 mA from a $2.4V$ supply.

Chapter 6

InP HBT E-band Power Amplifier Design

This chapter concentrates on design of indium-phosphide HBT based power amplifier MMIC for potential application in E-band communication systems operating in the frequency range 71-76 GHz. Introductory considerations concerning the capabilities of a single $10\times1.5\ \mu m^2$ HBT connected in common-emitter (CE) configuration, have been outlined in section 5.2. Here the maximum power gain and the stability factor of the CE stage will be compared to those of the common-base (CB) and the cascode stages. The CE configuration was selected for the power amplifier design as the only solution exhibiting unconditional in-band stability.

Multi-finger devices are normally used for high-frequency InP HBT power amplifier designs. Such unit-transistor cells were not available in the used process. The four-transistor power cell containing four combined single-finger $10\times1.5\ \mu m^2$ HBTs was therefore developed. Equal combining characteristics and equal loading of each HBT are important prerequisites for optimal utilization of a power cell [194]. Like all the other networks of the amplifier chip, the power cell passive structure was simulated using ADS electromagnetic simulation program, Momentum. Circuit simulations of the power cell with embedded HBTs will reveal uniform combining characteristics and HBT loading.

The common-emitter connected HBTs designed for mm-wave applications have tendency to oscillate at lower frequencies where their power gain is higher. The parasitic oscillations can cause distortion by modulating the desired signals. Great care was put on the stabilization of the amplifier. This chapter will describe simulation methods applied for detection of even-mode oscillations as well as their elimination by use of resistors in the bias circuitry. A suggested simulation method applied to predict and eliminate odd-mode oscillations in the PA chip will be presented as well.

This chapter will furthermore describe the operation and performance of the developed power MMIC. Input/output return loss and gain of the amplifier chip were measured under small-signal drive. The experimental setup will be outlined and the measured data will be presented along with the simulated ones. The simulated power and power added efficiency will represent record performance levels for an InP HBT power amplifier operating above $50GHz$. This InP HBT power amplifier is a first two-stage solution demonstrated in that technology in the 50-140GHz range.

6.1 Transistor Configuration

Millimeter wave HBT power amplifiers are mostly implemented in common-base (or grounded-base) [70, 73, 195] and cascode transistor configurations [83, 96, 195]. These configurations are suitable for mm-wave power amplifiers, because they provide higher gain as compared to common-emitter and common-collector HBTs. Single-stage InP HBT amplifiers have demonstrated 3.5 dB gain at 255 GHz in CE topology [196] and 7 dB gain at 176 GHz in CB topology [70]. Unlike the common-emitter amplifiers, the CB amplifiers are operated in a potentially unstable frequency region. Circuit stability requires therefore special attention in the CB designs. In the potentially unstable frequency range, maximum stable gain (MSG) is a figure of merit of an HBT. The common base MSG can be significantly lowered by the effect of layout parasitics including base access inductance and collector-emitter external capacitances [70, 73, 197]. If not accurately

modeled, these parasitics can also introduce uncertainty in the stability analysis of the CB amplifiers [70, 73]. This problem is, however, not so severe in CE amplifiers. Inductance in series with the emitter can actually deteriorate the gain of the CE connected device. This problem is however naturally solved by direct connection of the emitter to the coplanar ground planes. Connection of the emitter to the large metal planes will also improve removing the heat generated in the HBT, as it will be discussed in the next section.

A cascode is a two-transistor configuration composed of a common-emitter stage followed by a common-base stage. It requires less chip area per unit gain, as compared to CB and CE topologies. A cascode is, moreover, considered to have better thermal stability as compared to the single-transistor topologies [96,198]. Cascode gain can be severely reduced by a parasitic inductance of the decoupling capacitor in the base of the CB stage [96]. As in the case of CB amplifiers, the stability of the cascode cell is one of the essential design issues. Resistive terminations at the input/output of the mm-wave HBTs are commonly required to avoid the parasitic oscillations [83, 96, 199].

Basic gain and stability properties of the used InP HBT connected in CE, CB and cascode configurations were investigated using ADS simulator and the HBT model presented in the section 3.4.1. The three simulated configurations including biasing details are shown in the Fig.6.1. With the aim of comparison the HBTs were biased at same operating conditions, 20 mA collector current and 2.4 V collector-emitter voltage. The resistor R_{stab} serves to stabilize CB and Cascode stages. In following, performance of the three HBT configurations will be compared before and after insertion of R_{stab}.

An unconditionally stable amplifier stage has a Rollet's stability factor K larger than unity, and a positive stability measure [172]. If R_{stab} was not inserted in CB and Cascode, only the CE stage behaved unconditionally stable, with $K \simeq 2$, in the frequency band of interest 71-76 GHz, as shown in Fig.6.2. The CB HBT appears to be potentially unstable in practically whole frequency range up to 150 GHz. The gain and stability factor calculated in ADS at the center frequency 73.5 GHz are collected in the Table 6.1. The stability measure (not shown) was positive for all amplifiers after R_{stab} was inserted

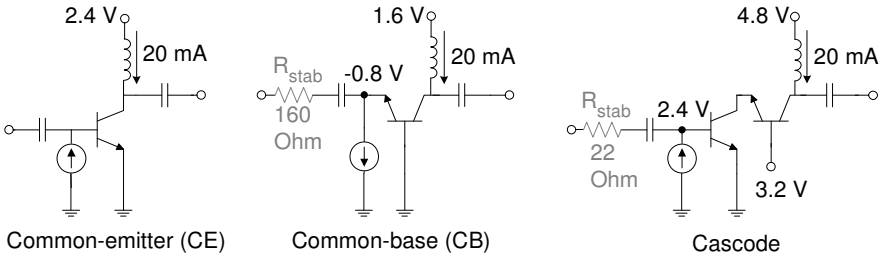

Figure 6.1: Simulation setups for the investigated transistor configurations including biasing and stabilizing details.

in CB and Cascode. Since the CE stage was unconditionally stable, its power gain is given as a maximum available gain (MAG) [172]. It can be concluded from the table that the common-emitter MAG is substantially lower as compared to MSG of the CB and the cascode connected HBTs, before R_{stab} was inserted.

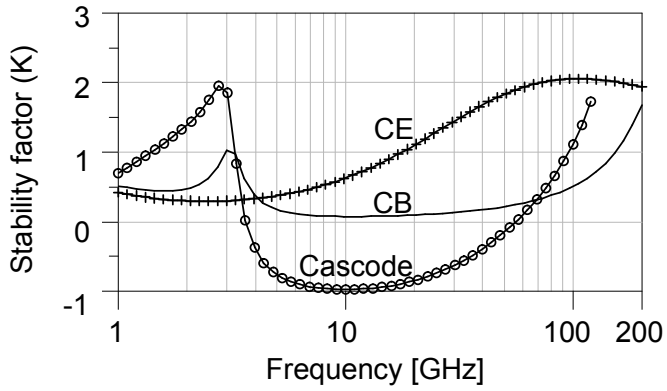

Figure 6.2: Simulated K-factor for the investigated transistor configurations from the Fig.6.1, without R_{stab} inserted.

To obtain the same level of stability (K=2 at 73.5 GHz) the resistors were inserted at the input of the CB and the cascode HBT as shown in the Fig.6.1. As a result, power gain of the CB stage reduced to 4.1 dB, which is more than 2 dB below the gain of the CE stage. The power gain of the cascode amplifier also reduced substantially, to 15.9 dB. However, the cascode gain remained superior.

	CE	CB	Cascode
MAG (MSG),without R_{stab}	6.3 dB	(9.5 dB)	(21.5 dB)
K @ 73.5 GHz	2	0.3	0.4
R_{stab}	%	180	22
MAG, with R_{stab}	%	4.1 dB	15.9 dB

Table 6.1: Stabilizing resistance and simulated data at 73.5 GHz for the three configurations from the Fig.6.1.

In this work, the two-stage high-power amplifier was implemented in the CE topology. The achievable gain of the HBT was thereby sacrificed to ensure in-band stability, and to avoid complications in the layout arising from a need for resistive loading of the HBTs in the CB and the cascode solutions.

6.2 Power Cell

As mentioned in the section 5.2, eight parallel-connected 10×1.5 μm^2 HBTs generate around 20.4 dBm output power at 1dB compression point. Large millimeter-wave HBTs typically have multiple emitter fingers connected in parallel. In the used process there was no dedicated multi-finger power cell. A power cell consisting of four one-finger transistors, shown in the Fig.6.3, was therefore developed as a building block for the design of the amplifier stages. Two of such cells provided the wanted output periphery of 120 μm^2.

6.2.1 Thermal Considerations

A single-finger device dissipating power is subject to self-heating arising from the finite thermal conductivity of the substrate. In multi-finger HBTs, a thermal coupling between the individual fingers results in elevated finger temperature, relative to the temperature of the single-finger case [200]. This limits the lifetime and power performance of the device. The power cell, depicted in the Fig.6.3, was designed to maintain low temperature in the four transistors. To obtain low thermal coupling through the substrate, the individual fingers were separated by 40μm [201]. Large metal planes surrounding the devices

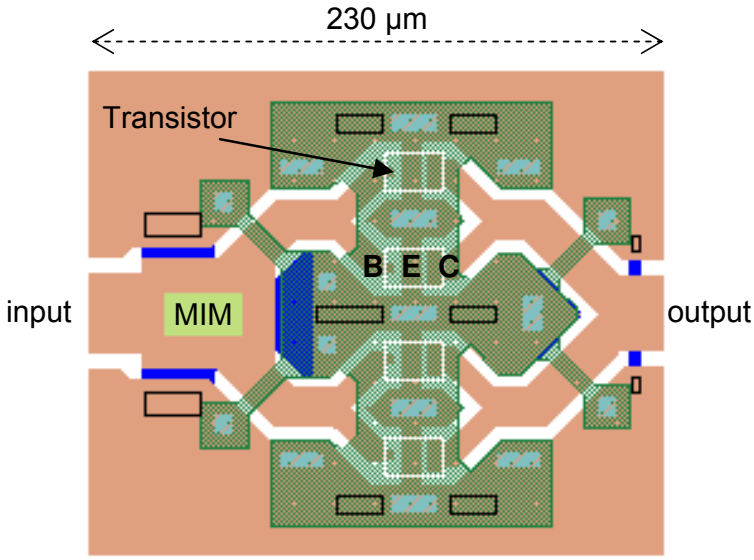

Figure 6.3: Layout of the power cell containing four $10\times1.5\ \mu m^2$ HBTs.

act as heat spreaders. The heat spreaders decrease the device temperature by transporting the heat from the emitter posts to the cool regions of the substrate. This technique can significantly improve the self-heating characteristics of the device [201, 202]. Central devices of a multi-finger cell can be expected to be mostly affected by the thermal coupling [200]. The two central ground planes help removing the temperature from the two central devices.

6.2.2 High-frequency Behavior of the Power Cell

Behavior of the passive structures of the power cell was analyzed using Momentum electromagnetic simulator. The calculated 14-port matrix was then imported in Agilent ADS for circuit simulations. To facilitate the construction of the power amplifier matching circuits, the power cells are pre-matched at the input by use of $\sim 0.3pF$ MIM capacitors, as indicated in the Fig.6.3. The four emitters are connected to the top metal plate by vias, located on both sides of the transistors. This eliminates undesired inductance in series with the emitters, therefore preventing gain degradation. The two central ground-planes,

connected by the air-bridges to the outer ground planes provide additional grounding for the two innermost transistors. This prevents that the top metal acts as a common lead for all the emitters.

In a well behaved power cell all transistors should operate equally. This implies equal combining characteristics and equal load impedance for each transistor [194]. The combining characteristics of the power cell were first verified in ADS simulator by comparing S-parameters of two different arrangements. In the first arrangement, only two outer transistors were connected in the passive power cell multi-port. In the second arrangement, only two inner transistors were connected. The results of the two simulations are plotted in the Fig.6.4. The cell behaves practically the same regardless of the transistor group used, and well beyond the E-band frequency range 71-76 GHz.

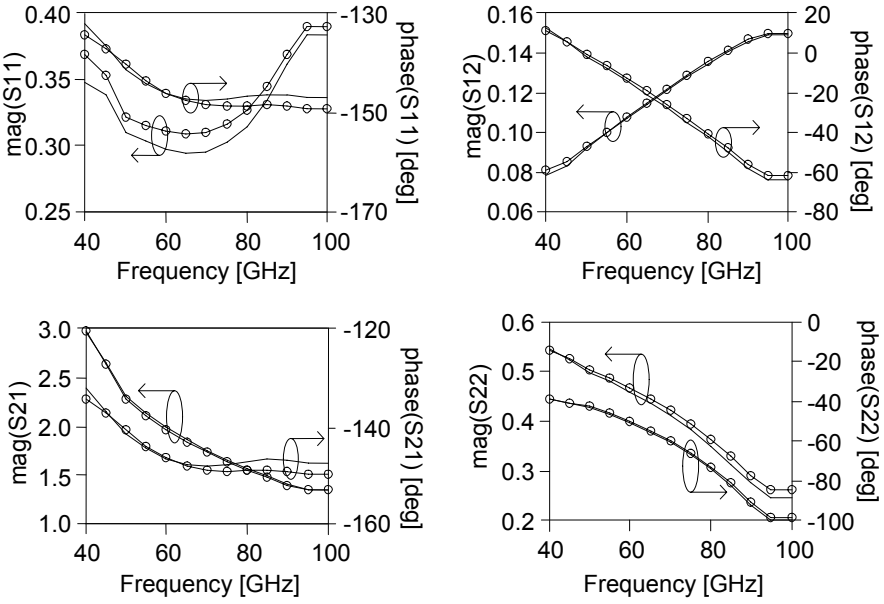

Figure 6.4: Comparison of the simulated S-parameters for the two arrangements in which only the two outer HBTs (-o-) and only the two inner HBTs (-) were connected to the power cell passive structure.

Another simulation was performed to verify the load impedance presented to the transistors. Here all four transistors were embedded in the cell multi-port. The cell was terminated by $(8.5+j8)\ \Omega$, aiming

to provide the optimum load impedance $(49+j30)\ \Omega$ to each transistor, which will enable the transistors to deliver a high output power, as mentioned in the section 5.2. At the input, the cell was driven by a voltage generator having impedance $(10.9+j0.7)\ \Omega$ providing minimum input reflection. The impedance seen by the outer and the inner transistor outputs became, $(47.5+j29.5)\ \Omega$ and $(51+j31)\ \Omega$, respectively, which is very near the optimum impedance. In fact, the two obtained load impedances lie inside a $0.05dB$ load-pull contour simulated and plotted on Smith-chart.

In reference [194], uniformity of an X-band FET power cell has been improved by employing asymmetric combiner layouts. The asymmetry has been introduced in form of slits and by adjusting the line widths [194]. In this work no such adjustments were necessary. The results presented in this section suggest an equal transistor operation in the developed power cell.

6.3 Amplifier Circuit

As depicted in the Fig.6.5 the amplifier is based on a driver stage and a high-power stage. Each stage was constructed using the two pre-matched 4-transistor power cells. The input of the driver stage was matched using small-signal impedance levels for minimum small-signal reflection. On contrary, the output of that stage was matched for high power output, to avoid premature power-gain compression in that stage.

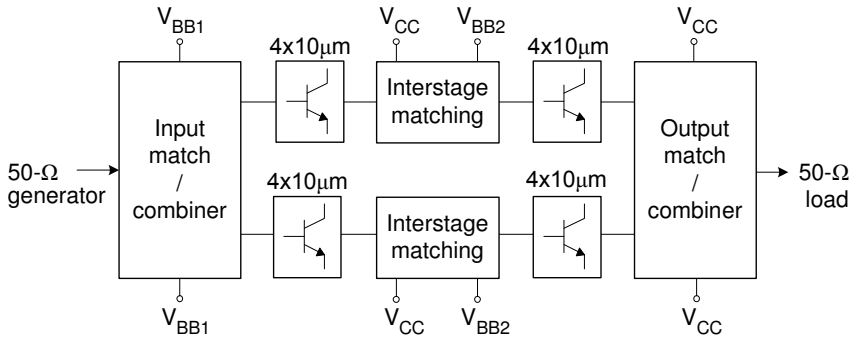

Figure 6.5: Block-diagram of the developed power amplifier.

When selecting the driver stage periphery, engineering trade-off exists between the power added efficiency and the driver's output power capability, as discussed in section 4.4 dedicated to the GaN HEMT amplifier design. In this amplifier, the ratio between the two peripheries, 1/1, is much higher as compared to the periphery ratio of the GaN HEMT amplifier, which is 1/2.7. Such large driver periphery is required because of the relatively low gain of the mm-wave HBT, which is 6.3 dB at 73.5 GHz. The periphery ratio of 1/1 provides a driver circuit saturating at high power levels, improving linear operation as required in communication systems. According to the ADS simulations of the amplifier circuit, the driver-stage HBTs are backed-off by 3.6 dB, when the power stage is in $1dB$ compression.

An apparent advantage of having two separate power cells in the driver stage is the combiner-less interstage matching circuit. Absence of an additional combiner reduces losses between the two stages, thus relaxing the demand for high-power capability of the driver stage. As illustrated in the Fig.6.6, the signal is split at the input of the driver stage instead, where the power dissipation is of no importance for the driver stage linearity.

The coplanar waveguides in the impedance matching circuits are illustrated using the thick lines in the circuit diagram in Fig.6.6. Complete schematic and component values can be found in Appendix B. Like the HBT power cells, all the networks were electromagnetically simulated using Momentum software.

Series coupling capacitors C_{s1}, C_{s2} and C_{s3} isolates the DC-bias of the two stages from each other as well as from the external 50Ω equipment. At the same time, the three MIM capacitors serve for impedance transformation in the matching networks. On the other hand, quarter-wavelength stubs, shorted at one end, act as nearly open circuits. Numerous air-bridges (not shown in the schematic), connecting the ground planes along all the CPW lines, and across the junctions and bends, were used to suppress slot-line mode excitation [203]. The parasitic effects of the air-bridges have significant influence on the impedance transformation in the matching networks.

The "Bias and stabilizing" boxes in the circuit diagram of the Fig.6.6 contain passive networks for AC/DC decoupling and even-

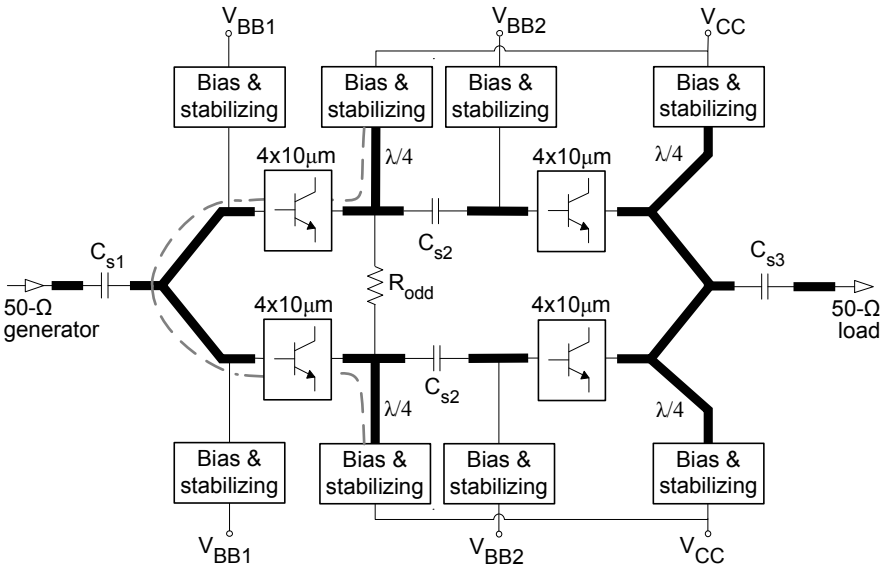

Figure 6.6: Conceptual diagram of the InP HBT power amplifier chip.

mode stability improvement. The resistor R_{odd} dampens the potential odd-mode oscillations. The circuit stability will be discussed in the next section.

As mentioned in section 5.2, the 320Ω resistor placed in series with the base supply voltage prevents thermal runaway of the single HBT. The four-transistor cell requires four times smaller resistor, 80Ω, to obtain the same DC-characteristics. The 80Ω stabilizing resistor R_b is inserted in the supply path of each power cell as illustrated in the Fig.6.7 (left plot).

6.4 Stability Analysis

6.4.1 Even-Mode Stability

Schematic of the "Bias & stabilizing" networks inserted in the base bias lines of the two stages is illustrated in the Fig.6.7 (left plot). It will be shown in this section that the 80Ω resistor R_b, used for base biasing, also improves even-mode stability by preventing potential low-frequency oscillations in the bias circuitry of the amplifier chip.

The L_B-C_{Ba} low-pass network prevents RF signal power dissipation in the resistor, and at the same time it allows undesired low-frequency oscillations to be damped by the resistor.

The collector biasing circuitry shown in the Fig.6.7 (right plot) also contains a stabilizing resistor. Here, however, this resistor was not placed in series with the supply lines, in order to avoid DC-power dissipation as well as modulation of the collector bias voltage by the signal envelope. The capacitor C_{Ca} of about 1.2 pF terminates the quarter-wavelength stub by low reactance. In the lower GHz range, however, the current is also allowed to flow through the order of magnitude larger C_{Cb}, and as a result, the power can be dissipated in the resistor. In following, the methods of amplifier stability analysis will be explained.

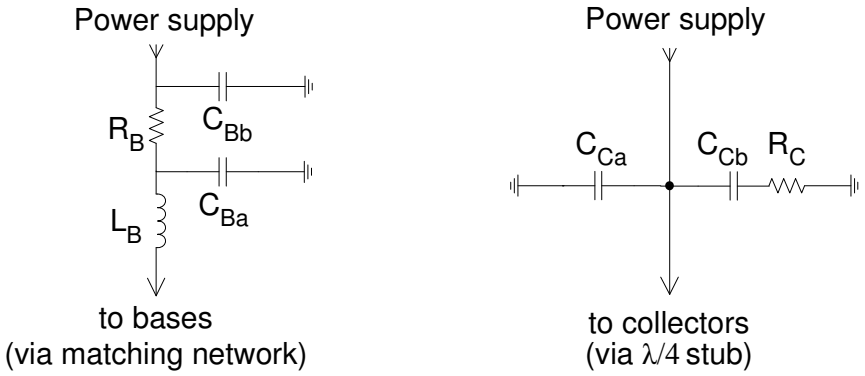

Figure 6.7: Circuitry for bias and low-frequency stabilizing of the amplifier stages. The entire amplifier circuit and component values can be found in Appendix B.

It is well known that inappropriate terminations in bias circuitry can cause low-frequency oscillations to occur [169]. Stability analysis was firstly performed by applying the test ports to the bias terminals of the amplifier, as suggested in reference [169]. The three bias lines V_{BB1}, V_{BB2} and V_{CC} respectively, appear in the both half-parts of the MMIC amplifier. For the stability analysis, the bias lines from the upper half-part were connected to those in the lower half-part, as shown in the Fig.6.8. Underlying assumption in this approach is that the two amplifier branches operate in even mode. To simulate the

stability of the power stage, the test ports were applied to the supply terminals V_{BB2} and V_{CC} as indicated. The driver stage was tested by moving the Port 1 to V_{BB1}.

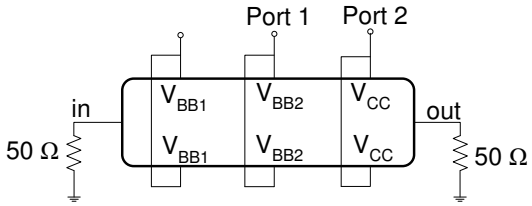

Figure 6.8: Setup for K-factor simulations with test ports connected to the bias lines.

In this analysis the driver stage showed unconditional stability, however K-factor was only about 1.2 in the sub-GHz range. The power stage turned out to be potentially unstable, with K-faktor falling below unity in frequency range 1.3-6 GHz, as indicated in the Fig.6.9.

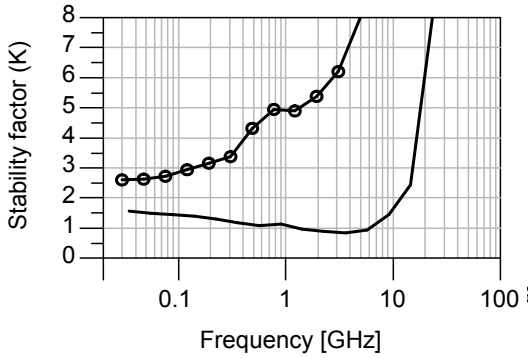

Figure 6.9: K-factor simulated in the setup from the Fig.6.8 before (-) and after (-o-) inclusion of the stabilizing resistors.

Input and output stability circles obtained at 3 GHz are plotted in the Fig.6.10. The regions inside the circles indicate ranges of impedances that will cause oscillations, when applied to the corresponding bias lines. Position of the stability circles on the Smith-chart suggests that large bypass capacitors in series with parasitic inductances, could give rise to the parasitic oscillations.

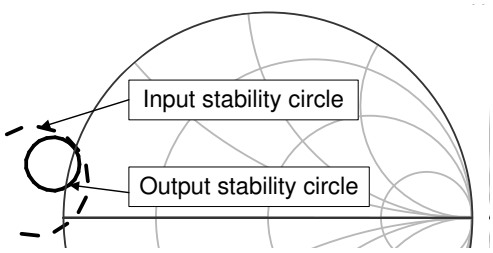

Figure 6.10: Input and output stability circles simulated in the setup from the Fig.6.8 at 3 GHz.

The potential instability could be eliminated by applying any of the two resistors, indicated in the Fig.6.7, in the bias circuitry of the power stage. The improvements in K-factor were, however, most prominent when both resistors were included. The stabilizing circuits with same topology were adopted also in the driver stage to further enhance its minimum K-factor to 2.8. The K factor of the power stage improved to above 2.5 in the entire frequency range $30MHz$-$100GHz$, as shown in the Fig.6.9.

Occurrence of the oscillations was further investigated by connecting the test ports to the input and output of the power amplifier. The amplifier chip appeared to be unconditionally stable with minimum K-factor of 1.6 at 12 GHz. Outside the 6-18GHz band, the K-factor was larger than 9.

Ensuring that the overall amplifier is resistant to the oscillations by using the input and output as the ports is necessary but not sufficient to guarantee the stability. In principle, the two amplifier stages can still oscillate, because they act as active loads to each other. Therefore a stability test was carried out to analyze the two stages separately. The power amplifier was partitioned at the output of the driver stage power cells. The two outputs of the driver stage cells were then connected together to obtain a single output port of the driver stage. Similarly, the two inputs to the interstage matching networks were connected together to obtain a single input to the power stage. The power stage turned out to be unconditionally stable in this test, while the driver stage showed potential instability in frequency range 2.6-11 GHz. The stability of that stage was therefore carefully investigated

using the mapping circles calculated at the power-stage input. The mapping circles calculated in ADS represented contours of impedances seen into the input of the power stage, when its output was terminated by a range of impedances lying on unity-magnitude reflection circle. Results of this simulation are illustrated in the Fig.6.11. It can be concluded from the figure that there is no overlap between the output driver-stage stability circles with the power-stage mapping circles. Hence, the driver stage remains stable for any passive load applied to the output of the amplifier chip. The same kind of test was performed by using the bias lines as the output ports for the power stage. Neither in this case the two groups of circles overlapped. Using the same approach, it was finally also ensured that the input stability circles of the power stage do not overlap the mapping circles of the driver-stage output.

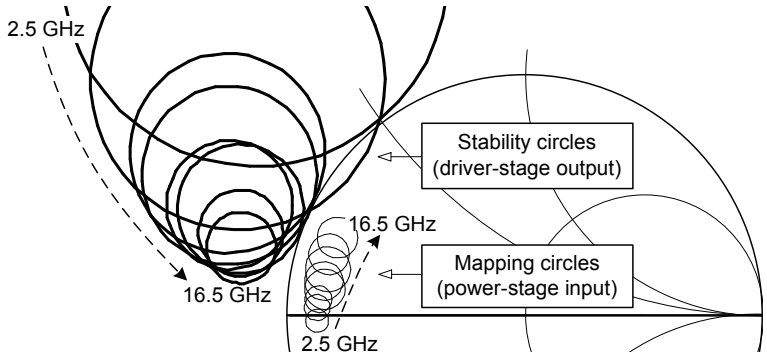

Figure 6.11: Output stability circles of the driver stage and input mapping circles of the power stage to test the driver stage stability. The simulation results are presented for the frequency range 2.5-16.5GHz in a 2GHz step.

6.4.2 Odd-Mode Stability

Another stability test was performed such that the two amplifier branches were excited in odd mode and oscillations were observed. Fig.6.12 illustrates the simulation setup in which Transient Simulation tool in ADS was used. The two voltage sources each generate a single pulse with opposite polarity to excite the oscillations in the odd-mode.

If the oscillations decrease with time and vanish, the circuit is regarded to be stable to this mode. The results of such a study are presented in Fig.6.13, where the voltage time waveforms in the two amplifier branches are shown as a function of time. It can be seen that without the stabilizing resistors, an odd mode oscillation will potentially develop and will lead to strong oscillations at about 11.7 GHz. Introducing a 10Ω resistor R_{odd} eliminates the instability problem.

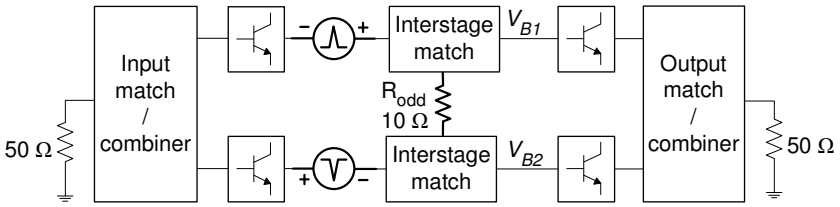

Figure 6.12: Setup for time-domain simulations of the odd-mode oscillations.

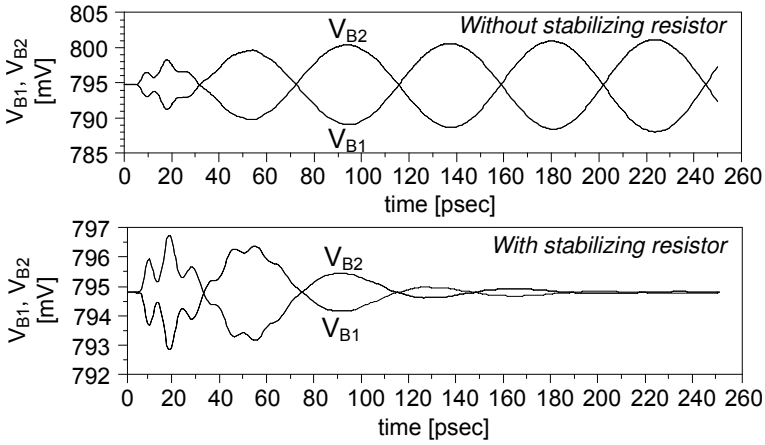

Figure 6.13: Time evolution of an odd-mode excitation to test the stability of the amplifier.

It should be pointed out that only the driver stage was responsible for the odd-mode instability. The unstable operation was namely obtained even if the power stage cells and output combiner were removed from the simulation setup. The oscillation loop in the driver stage is actually formed by the two power cells, the input power split-

ter and the two stubs. This loop path is indicated by the dashed line in the Fig.6.6). On contrary to that, the power stage behaved stable, if the driver cells were removed. Input side of the power stage sees the $209fF$ blocking capacitor C_{s2} and the lossy bias network, which damps the oscillations in that stage. As a result, the R_{odd} was only effective in damping the oscillations if inserted in the circuit on the left hand side of the C_{s2}, as it was shown in the Fig.6.6.

6.5 Amplifier Performance

Photograph of the circuit fabricated in the InP HBT coplanar process from Alcatel-Thales III-V Lab is shown in the Fig.6.14. The circuit was laid out symmetrically around horizontal center-axis to assure equal operation of the two half-parts. The chip area measures $1.45 \times 1.25\ mm^2$.

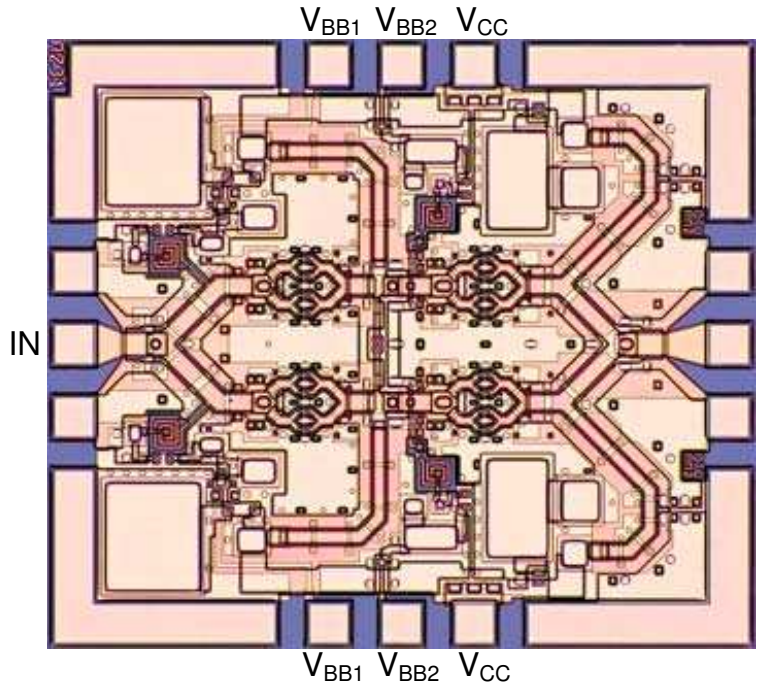

Figure 6.14: Photograph of the InP HBT two-stage power amplifier MMIC.

On-wafer S-parameters of the power amplifier were measured using an Anritsu ME7808B Broadband Vector Network Analyzer (VNA), and 110GHz coaxial probes, as illustrated in the Fig.6.15. Ground-signal-ground (GSG) Infinity Probe was used for contacting the amplifier's input pad, while the output was contacted with the Picoprobe. DC-power was applied to the MMIC using power probes.

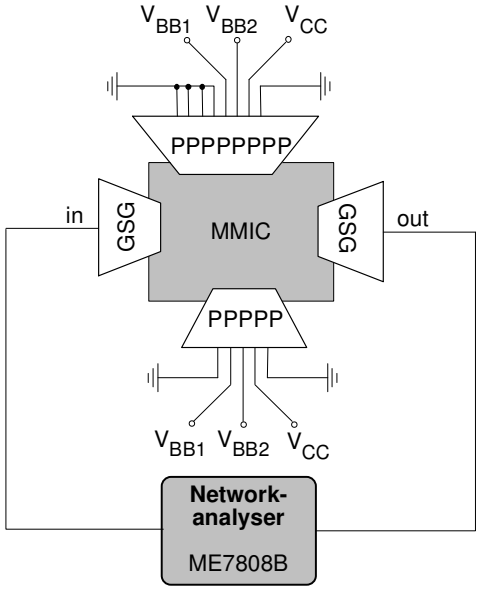

Figure 6.15: S-parameter measurement setup.

Measured small-signal gain and input/output return losses are compared with the data predicted by ADS in the Fig.6.16. The data were obtained at total collector current 320 mA and collector voltage 2.4 V. From the measured S21 magnitude it can be concluded that the 3dB bandwidth is 60-95GHz, which is equivalent to 45% relative bandwidth. The input matching network was optimized in simulations to yield minimum reflection at the center frequency 73.5 GHz as indicated in the Fig.6.16. The measured return losses are, however, significantly shifted upwards in frequency compared to the simulated ones. Maximum value of S21 magnitude therefore also occurs at higher frequency than predicted. The simulated and measured S21 have peak values of 10.4 dB at 68 GHz and 7.5 dB at 77 GHz respectively. The

relatively low value of the measured peak value of S21 is partially caused by the the fact that the S21 of the used HBT decreases by about $1dB$ from 68 GHz to 77 GHz. The discrepancy between the simulated and measured return losses and gain could moreover stem from the inaccuracies in the Momentum simulations of the passive structures and sensitivity to the process variations.

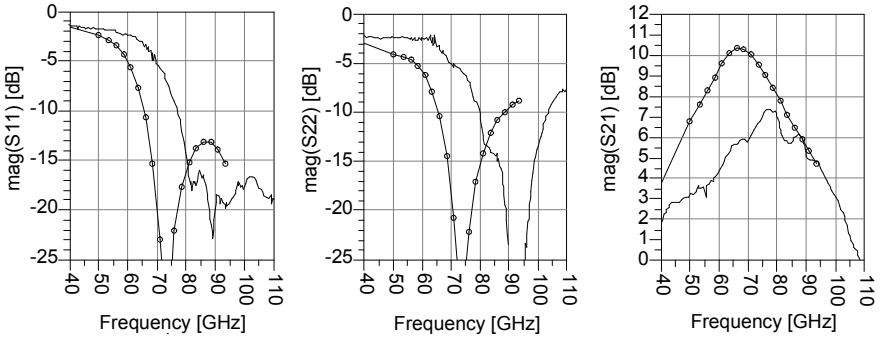

Figure 6.16: Comparison between the simulated (-o-) and measured (-) input/output return losses and gain magnitude.

The simulated output power versus input power is illustrated in Fig.6.17 together with the power-added efficiency and gain characteristics. The power amplifier MMIC achieved an output power in excess of 20 dBm. The $1dB$ compression point power level is just below 20 dBm resulting in P_{1dB}=19.6 dBm. It can be concluded from the figure that the power-added efficiency peaks at around 15% around the saturation point and is higher than 10% at $1dB$ compression point.

Deviation between measured and simulated S22 in the Fig.6.16 indicate the possibility that the power-stage transistors might not be optimally loaded. This will eventually cause degradations in output power and PAE values predicted above. Owing to lack of equipment, large-signal measurements of the power MMIC were not possible.

6.6 Discussion

A two-stage InP HBT high-power amplifier was developed based on common-emitter topology. Potential instability in lower GHz range

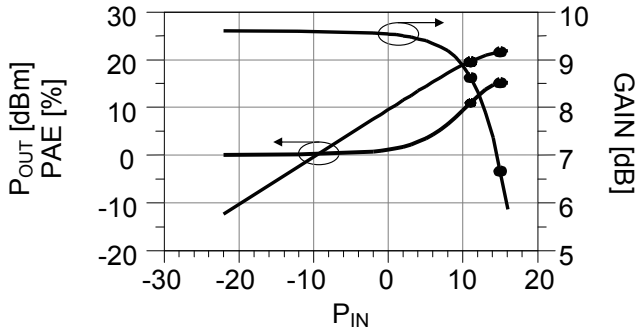

Figure 6.17: Simulated output power, PAE and transducer gain for the power amplifier MMIC at 73.5 GHz.

appeared in the bias-line analysis. Insertion of resistive loadings in the bias circuitry resulted in minimum K of 2.5 in the entire frequency range, without compromising high-frequency gain. A method for simulation of the odd-mode oscillations between the combined transistors has been presented and successfully applied to stabilize the driver stage using a single resistor.

The developed four-transistor power cell provides nearly equal combining characteristics and load impedance to all four transistors. The amplifier exhibits a peak small-signal insertion gain of 7.5 dB at around 77 GHz. The gain falls by $3dB$ at $60GHz$ and $95GHz$. The measured return-loss characteristics were remarkably upward-shifted in frequency compared to the simulated ones, which also caused gain reduction. Whether these deviations arose from sensitivity to the process parameters or inaccurate modeling will be investigated in the future. Moreover, implementation of the CB or cascode configurations will be reconsidered more deeply aiming at higher gain per amplifier stage.

The simulated output power in $1dB$ compression is 95 mW or 19.6 dBm, while the saturated power is in excess of 100 mW. The achieved power added efficiency peaks at around 15% around saturation point. The reported results demonstrate the possibilities to utilize ATL InP HBT processes in the design of mm-wave power amplifiers. The achieved power and PAE data represent record performance levels from an InP HBT power MMIC operating above $50GHz$.

Chapter 7

InP HBT mm-wave QVCO design

Millimeter-wave systems such as E-band communication transceivers require high-performance oscillators for high-frequency signal generation. Quadrature voltage controlled oscillators are useful for quadrature (de)modulators, in direct-conversion transceivers and for image reject mixers. The previous two chapters of this thesis demonstrated applicability of ATL's InP HBT technology for design of millimeter wave PAs. Same technology was used to implement mm-wave quadrature voltage controlled oscillator, described in this chapter.

High-frequency QVCOs are mainly realized as two identical oscillators interconnected by coupling circuitry. The two oscillators can be realized as ring oscillators [204], taking up less die area and having wider tuning range as compared to LC-tank oscillators. However, superior phase-noise performance of the LC-oscillators makes them more attractive in many communication systems. The LC-oscillator concept was adopted in this work.

One way to realize frequency tuning in a LC-QVCO is to implement varactors [46, 205], as in the most single VCOs. Microwave [118] and mm-wave [206, 207] VCOs can suffer from low quality factor of the varactors and the associated parasitic capacitances that degrade phase-noise performance and diminish tuning range. An alternative solution for QVCO tuning is a variation of coupling factor between

the oscillators [45, 47]. Because high-quality varactors were not available in the used InP HBT process, variation of the coupling factor was adopted. Interaction of this tuning mechanism with bias-dependent capacitances of the HBTs will also be investigated.

Very high oscillation frequencies demanded by mm-wave systems necessitates miniaturization of LC-resonators [46]. High-frequency oscillator performance becomes therefore highly dependent on layout and transistor parasitics. In this chapter, parasitic effects of an interconnecting line inductance and of a base resistance will be analyzed in a feedback model of a cross-coupled mm-wave LC-oscillator. The analysis will also encompass a resonator, which is intentionally isolated from the device using an additional capacitor. This technique is commonly applied in cross-coupled mm-wave oscillators [117, 119] and also in lower microwave range [118].

A simple cross-coupled differential oscillator architecture has been successfully implemented in a CMOS-based mm-wave VCO [206] as well as in a QVCO [45]. However, a mm-wave QVCO based on this architecture, further in this text referred to as 'simple' architecture, has not yet been demonstrated in any bipolar technology. A $28GHz$ SiGe HBT QVCO [49] was based on a cross-coupled topology, which includes an additional emitter-follower transistor pair in the feedback path of each oscillator. A possible advantage of this 'buffered' approach is a separation of the resonator from the transistor parasitics, which could enhance the achievable oscillation frequency and improve phase-noise. However, an additional loop-delay and noise introduced by the emitter followers might have negative impact on the performance. Moreover, capacitively loaded emitter followers might become unstable [208], which could cause parasitic oscillations in a QVCO.

This chapter explores properties of the 'simple' and the 'buffered' oscillator architectures, based on the used InP HBT process. The two single oscillators will firstly be treated using feedback theory. The analysis and linear simulations will be performed based on their simplified small-signal equivalent circuits. From these results, behavior of QVCOs based on the two oscillator types will be inferred. Non-linear device models will then be employed to verify the performance of the two QVCOs in a nonlinear simulator. Potential instability risk due to

the buffers in the feedback path will be investigated. The implemented QVCO design based on the buffered topology will be presented, along with the experimental results and the procedures applied to verify the achieved tuning range and power performance.

7.1 Principle of Operation of a QVCO

Block diagram of the realized QVCO is shown in the Fig.7.1. Barkhausen criterion imposes the phase-shift around an oscillator loop to be zero or integer multiple of 360° at the oscillation frequency. To fulfill this requirement, phase offset between the differential outputs of the two identical oscillators has to be 90°, and one of the outputs has to be inverted, as indicated in the figure.

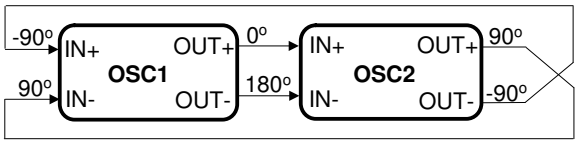

Figure 7.1: Block diagram showing two identical oscillators coupled in a QVCO loop.

QVCOs employing simple oscillator topology from the Fig.7.2 (left) as the building block, has been subject of theoretical analysis by several authors [209–212]. The simple QVCO has been described as a chain of transconductors followed by parallel RLC-networks connected in a loop. The cross-coupled pair of the core transistors T_{cr}, and virtual ground existing between their emitters ensure differential operation. The output transistors T_{out} serve to drive 50Ω equipment. Coupling transistors T_{cp} provide coupling from another identical oscillator. Quadrature generation is established by connecting the IN± and OUT± terminals of the two oscillators in a manner described by the Fig.7.1. As a result, T_{cr} and T_{cp} transistors are excited by base-emitter voltages which are 90° out of phase. Thus, the signal currents, i_{cr} and i_{cp}, generated by the two respective transistors, are in quadrature as well, as depicted in the Fig.7.2 (right). Magnitudes of the two currents are proportional to the fundamental components

of the respective large-signal transconductances $G_{m,cr}$ and $G_{m,cp}$. Total current i_{tot} injected into the resonator is equal to $i_{cp} + i_{cr}$. In this simplified analysis it was assumed that the resonator can be represented by a parallel RLC-network (resistor is not shown), and no current flows into the base of another transistor. This detail will be included in the analysis in section 7.2.

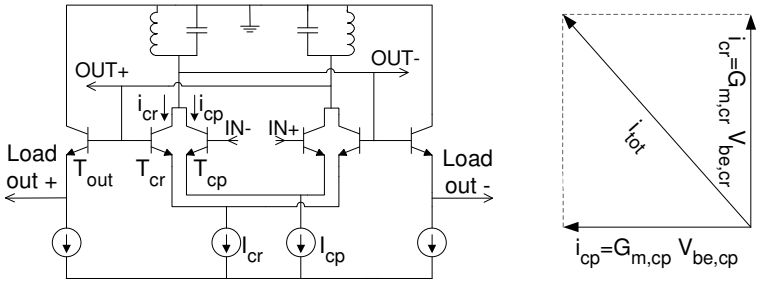

Figure 7.2: Left: Conceptual diagram of a simple cross-coupled oscillator, as a building block of a QVCO. Right: A phasor representation indicating signal currents in the devices.

A single oscillator operates at resonance frequency of the LC-tank, where the phase of its impedance function is zero. Because i_{tot} is phase-shifted as compared to the single oscillator case, the QVCO has to operate away from the tank resonance to maintain zero-phase shift around the loop. This frequency departure increases with the transconductance ratio

$$m = \frac{G_{m,cp}}{G_{m,cr}} \tag{7.1}$$

which has been defined as a coupling factor of a QVCO [209]. Frequency tuning can be be accomplished through variation of DC-currents I_{cr} and I_{cp} that control the two respective transconductances.

In an oscillator that do not oscillates at the resonance frequency of the LC-tank, phase $\Delta\varphi$ of the tank impedance function at the oscillation frequency ω_0 would not be zero. Near the resonance $\Delta\varphi$ is small, and an effective resonator quality factor Q_{eff} can be estimated from the slope of the phase characteristic $d\varphi/d\omega$ at ω_0 [213],

$$Q_{eff} \simeq \frac{\omega_0}{2}\frac{d\varphi}{d\omega}. \tag{7.2}$$

Because the phase slope is steepest at the resonance frequency, Q_{eff} decreases with increasing phase deviation $\Delta\varphi$. For large values of $\Delta\varphi$, approximation to the Q_{eff} is [214]

$$Q_{eff} \simeq Q\cos(\Delta\varphi). \tag{7.3}$$

where Q is quality factor at the resonance frequency. Again it follows that Q_{eff} decreases as $\Delta\varphi$ departs from zero.

Leeson's equation (3.2) showed that LC-oscillators benefit from high Q with regards to the phase noise. Hence, the phase noise of a single oscillator increases as the oscillation frequency departs from the resonance frequency. The same is true for quadrature oscillators. Phase-noise in the simple model of a QVCO, based on a parallel RLC-tank, differs by factor $[1 + m^2]/2$ from the single oscillators phase-noise [209], where m is given in the eq.(7.1).

7.2 Small-Signal Approximation of the Simple Oscillator

The simple cross-coupled oscillator topology from the Fig.7.2 have been successfully exploited in a $43GHz$ CMOS QVCO, tuneable by a bias-dependent coupling [45]. This section explores the performance limiting factors of an HBT-based simple oscillator operating in a QVCO. Open-loop equivalent circuit of the oscillator will be developed based on small-signal equivalent representation of the used InP HBT and the resonator circuit. The equivalent circuit will identify main limitations of the transistor in the simple oscillator topology. After that, open-loop transfer functions will be derived for three oscillator circuits, in order to explain the impact of the base resistance, inductance of an interconnecting line and an additional coupling capacitor, which can enhance the loop gain and the oscillation frequency. Finally, an open-loop simulation will be performed on the equivalent circuit.

7.2.1 Simplified Equivalent-Circuit Representation

A closed-loop equivalent circuit representation of the simple oscillator, illustrated in the Fig.7.3 a), is based on small-signal elements of the transistor and resonator circuit. Element values of the HBT, listed in Table 7.1, were extracted from the large-signal model of the device presented in [139]. Parallel connection of the elements L_r, C_{res} and R_r represents the inductor implemented in the QVCO, described in sections 7.4 and 7.5. The inductor elements were extracted using EM-simulation software Momentum. The R_r is omitted in the equivalent circuit since the overall Q is strongly dominated by the losses originating from the transistors, as will be explained shortly. The collector-emitter fringing capacitance C_{ce} is summed with C_r into a single element C_r as shown in the Fig.7.3 a). Contributions of the external region of the device to the total C_{bc} was 80%. To simplify the model C_{bc} was therefore applied externally as indicated.

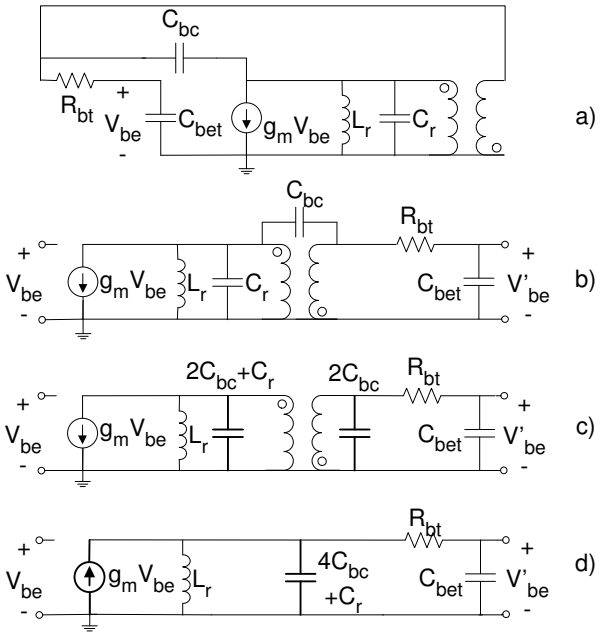

Figure 7.3: Transformation of the simple cross-coupled oscillator from the closed-loop a) to the open-loop representation b). Diagrams c) and d) are equivalent representations of the diagram b).

Parameter	*Value*			
	Passives	$I_c = 1mA$	$I_c = 3mA$	$I_c = 5mA$
$C_{bc}[fF]$		5.5	4	3.5
$C_{be}[fF]$		39	61	79
$R_b[\Omega]$		44	42	41
$g_m[mS]$		30	92	152
$C_{ce}[fF]$	7.9			
$L_r[pH]$	115			
$R_r[\Omega]$	849			
$C_{res}[fF]$	4.1			

Table 7.1: Small-signal element values of the $3 \times 1.5\mu m^2$ device biased at $V_{ce} = 0.8V$, and parasitics representing the resonator inductor at 50 GHz.

In the closed-loop model of the Fig.7.3 a), one half-part of the oscillator loop is represented by the extracted components, and another identical half-part by the ideal transformer having transformation ratio $N = -1$. This representation is valid because the voltage waveforms across the two inductors in the Fig.7.2 are 180° out of phase.

The transformer output looks into the base terminals of the core transistor T_{cr}, coupling transistor T_{cp} in another oscillator, and the output buffer T_{out}. Since same bias is assumed for the three transistors, their C_{be} and R_b are same. Furthermore, the C_{be}-R_b networks of T_{cr} and T_{cp} appear to be in parallel, since their emitters are at virtual grounds. Under assumption of unilateral T_{cr} and T_{cp} (neglecting their C_{bc}), their C_{be} and R_b were merged into single RC-network, $C_{bet} = 2C_{be}$ and $R_{bt} = R_b/2$, as shown in the Fig.7.3 a). This approach would not make sense in an equivalent circuit of a QVCO. However, purpose of this unilateral assumption is only to approximate the additional loading of T_{cp} on the resonator in a single oscillator of a QVCO.

Input admittance of the output buffer driving 50-Ω load is

$$Y_{in,T_{out}} = j\omega C_{bc} + \left(50 + R_b + R_b + \frac{1 + g_m(50 + R_b)}{j\omega C_{be}}\right)^{-1} \tag{7.4}$$

$$= j\omega C_{bc} + (102 + 1/(j\omega 0.15 C_{be}))^{-1}, \tag{7.5}$$

where emitter access resistance is $R_b = 10\Omega$ and values for R_b and g_m at $3mA$ from the Table 7.1 have been assumed. After insertion of the C_{be} and C_{bc} from the Table 7.1 into the eq.(7.5), it can be shown that the impedance $|1/Y_{in,T_{out}}|$ is order of magnitude larger than impedance of the R_{bt}-C_{bet} series network. Hence, relatively low signal current flows into the base of T_{out}. Therefore, it is not likely that T_{out} would significantly degrade the oscillation frequency. This was also proven by harmonic balance simulations of this oscillator, namely, oscillation frequency only increased by 4% after removing the T_{out}. It is moreover easily seen that the quality factor of the second term of the eq.(7.5), Q=$1/(102 \times 0.15\omega C_{be})$ is relatively high as compared to the Q of the dominating R_{bt}-C_{bet} network, Q=$1/(42\omega C_{be})$. Hence, oscillation frequency and total quality factor are dominated by the R_{bt}-C_{bet} network.

At the oscillation frequency of 50 GHz, the inductor Q was 23.5, which is around 19 times higher than Q of the R_{bt}-C_{bet} series network at $3mA$. Therefore, the inductor parasitic resistance is also omitted in the equivalent circuit.

In the Fig.7.3 b) the oscillator elements are rearranged such that the reference plane for opening the loop at the B-E junction becomes apparent.

After opening the loop, a Miller theorem was applied on C_{bc}. This component can be replaced by two equivalent capacitors of double size on each side of the transformer since

$$Y_{Mill,in} = j\omega C_{be}(1 - N) = j\omega 2C_{be} \tag{7.6}$$

$$Y_{Mill,out} = j\omega C_{be}(1 - 1/N) = j\omega 2C_{be}, \tag{7.7}$$

where $N = -1$. The obtained circuit looks like in the Fig.7.3 c). According to the theory from [215], the elements on the right side of the transformer having $N = \pm 1$ can be moved to the left side without changing their values. After $2C_{bc}$, R_{bt} and C_{bet} were moved to the left side of the transformer, the transformer was removed, and the current source has reversed direction in order to preserve the sign of the voltage transfer function. After these rearrangements the diagram becomes that depicted in the Fig.7.3 d).

When quadrupled by the Miller effect, C_{bc} grows into $20fF$ range and becomes comparable to C_{be}=$61fF$. C_{bc} would become even more harmful if placed in the intrinsic transistor since it would be charged through the R_b. In the present circuit it limits only the oscillation frequency, but main performance degradation comes from the large capacitance C_{be}, as well as $C_{be}R_b$ time constant, which governs the total Q of the oscillator. The quality factor of the $C_{be} - R_b$ network is 1.25 at $50GHz$.

Maximum oscillation frequency of a device, $f_{max} = \sqrt{f_t/(8\pi C_{bc}R_b)}$, is often regarded as the key parameter for high performance oscillator design. However, f_{max} can be high because C_{bc} is low - but R_b might still be high. Low C_{bc} would increase f_{max} also through the expression for the cut-off frequency given in the eq.3.6. Similarly, f_t alone is not a guarantee for a good phase-noise since it disregards R_b. Therefore, for a high performance mm-wave QVCO of this type, both FOMs must be high, and $C_{be}R_b$ time constant should be low.

7.2.2 Parasitic Effects and Modifications in a Resonator Structure

Simplified equivalent model from the Fig.7.3 d) will be extended here in order to explain influence of various parasitic elements and modifications that might occur in the simple type of oscillator. The extended version of the equivalent diagram, shown in the Fig.7.4, includes now also R_r, which is assumed to represent a resonator loss, and X_s which will either represent a parasitic inductance of an interconnecting line or a series capacitance, which serves to enhance the resonator Q. The R_s series resistor represents the base resistance. To simplify the analytical expressions, impact of the three elements will be analyzed separately, through three cases.

Case 1: $X_s = 0$ Assuming no series reactances, the open-loop transfer function can be written as

$$\frac{V_{be}^{'}}{V_{be}} = \frac{g_m}{\underbrace{R_s C_p \left(\frac{1}{L_r} - \omega^2 C_r\right)}_{G_{peq}} + sC_p\frac{R_s}{R_r} + \left(\frac{1}{sL_r} + s(C_r + C_p) + \frac{1}{R_r}\right)}. \tag{7.8}$$

where $s = j\omega$. The eq.(7.8) suggests that the passive elements could be represented by a parallel RLC-network at angular frequency ω. The rightmost term in the denominator in the parenthesis is an admittance, equivalent to the four shunt elements in the absence of the R_s. The second term is an additional capacitive contribution arising from R_s. First term is an additional equivalent conductance, G_{peq}, accounting for the losses introduced by R_s. Using the values from the Table 7.1, it follows that $R_s/R_r \simeq 0.05 << 1$. Hence, the second term represents a very small capacitance in comparison to the dominant $(C_r + C_p)$, meaning that R_s will not significantly slow down the oscillator. In the discussed simple oscillator, main loss comes from the base resistance R_s, and thus $G_{peq} >> 1/R_r$. Under these assumptions, the quality factor and the oscillation frequency can be estimated as

$$Q = \frac{1}{\omega_0 L_r G_{peq}} \qquad and \qquad \omega_0 = \left(\sqrt{L_r(C_r + C_p)}\right)^{-1}. \tag{7.9}$$

Substitution of G_{peq} from eq.7.8, into eq.7.9 yields

$$Q = \frac{C_p + C_r}{R_s C_p^2 \omega_0} = \frac{1}{\omega_0^3 R_s C_p^2 L_r}. \tag{7.10}$$

Assume now a device with given R_s and C_p. From the first expression in eq.(7.10), it follows that increasing the tank capacitance C_r, while keeping ω_0 constant, would increase the Q. This is only possible if the inductance is reduced. Same can be deduced from the second expression - trying to increase L_r, while keeping ω_0 and transistor parameters constant, would lead to reduction of Q. In other words, in a bipolar oscillator, if the base series resistance strongly dominates the overall Q, it is more beneficial to have large tank capacitance than a large inductance.

Another interesting detail in eq.(7.8) is that G_{peq} decreases with frequency. Due to that fact, peak in magnitude of the transfer function will be shifted up in frequency, away from the point where the phase crosses zero.

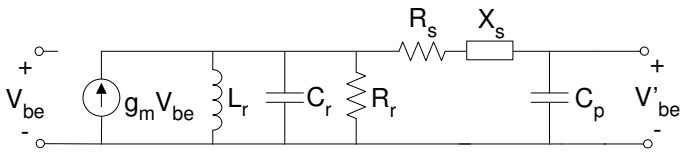

Figure 7.4: Open-loop equivalent circuit of the simple oscillator extended for analysis of various parasitic effects.

Case 2: $X_s = j\omega L_s$ will now be inserted in the circuit of Fig.7.4 to analyze impact of an interconnecting inductance L_s on the simple oscillator performance. Neglecting the small sC_pR_s/R_r term, as in Case 1, the transfer function becomes

$$\frac{V_{be}^{'}}{V_{be}} \simeq \frac{g_m}{G_{peq} + \frac{L_sC_p}{R_r} + sL_sC_p\left(\frac{1}{L_r} - \omega^2 C_r\right) + \left(\frac{1}{sL_r} + s(C_r + C_p) + \frac{1}{R_r}\right)}. \tag{7.11}$$

Again, in the absence of the parasitic element L_s, the parallel RLC term on the right side of the eq.(7.11) would determine the oscillation frequency ω_0. The third term represents an additional parallel susceptance coming from L_s. Possible new zeros in the phase response could be calculated by solving a 4^{th}-order equation. Most interesting is however the shift of ω_0 due to L_s. Since $C_r < C_r + C_p$, the third term is positive near ω_0, that is, the term represents an additional positive shunt capacitance, thereby reducing ω_0. Therefore, if a high oscillation frequency is desirable in the simple topology, base-terminals should be connected to the resonator circuit using shortest possible interconnects. This principle can also be applied to the other types of oscillators when connecting a large capacitance to the resonators.

The second term of eq.(7.11) accounts for the additional loss coming from L_s. The first term is the loss contribution from the base resistance, already described in eq.(7.8). It can be intuitively seen that L_s does not strongly influence the Q, since both the conductive

and the capacitive contributions from L_s (2^{nd} and 3^{rd} term, respectively) are proportional to L_s.

Case 3: $X_s = 1/(j\omega C_s)$. Transfer function of that version of the oscillator circuit, written in form compatible with the previous two cases, is

$$\frac{V_{be}^{'}}{V_{be}} \simeq \frac{g_m}{G_{peq} + \frac{C_p}{C_s}\left(\frac{1}{sL_r} + sC_r + \frac{1}{R_r}\right) + \left(\frac{1}{sL_r} + s(C_r + C_p) + \frac{1}{R_r}\right)}. \tag{7.12}$$

The small sC_pR_s/R_p term is again omitted for simplicity. As in the two previous cases, the rightmost term of the equation represent the admittance function in the absence of the series elements. The second term acts as an additional parallel RLC-network, and is proportional to $1/C_s$. The oscillation frequency is determined by the total capacitance across the L_r,

$$\omega_{0s} = \left(\sqrt{L_r\left(C_r + \frac{C_sC_p}{C_s + C_p}\right)}\right)^{-1}. \tag{7.13}$$

Small value of C_s offers several advantages with respect to high oscillation frequency and Q. First, oscillation frequency goes up and approaches $\omega_0 = 1/\sqrt{L_rC_r}$. Second, when the second and the third term of the eq.(7.12) are added, it is seen that the total equivalent inductance of the parallel circuit representation decreases, and total equivalent capacitance increases. Third, as the oscillation frequency ω_{0s} approaches ω_0, G_{peq} vanishes, as shown in the eq.(7.8). These three facts count towards higher total Q. Unfortunately, as C_s decreases, the $1/R_r$ term in the second term of the eq.(7.12) grows as well and becomes comparable to G_{peq}. For a very small C_s, the magnitude of the transfer function will be dominated by the $C_p/(C_sR_r)$, which can be seen as a magnified resonator conductance. A value of C_s at which the two conductances, G_{peq} and $C_p/(C_sR_r)$, are equal, is given by

$$C_s = \frac{L_r\left(C_r + C_p + \sqrt{(C_r + C_p)^2 + \frac{4R_sR_rC_pC_r}{L_r}}\right)}{2R_sR_rC_p}. \tag{7.14}$$

Below this value of the series capacitance, $C_p/(C_sR_r)$ conductance component will more and more rapidly degrade the magnitude of the transfer function.

7.2.3 Simulated Open-Loop Response

Frequency tuning mechanism of a QVCO based on the simple oscillator topology can be inferred from a plotted open-loop voltage transfer function of the single oscillator. For this simulation, a simplified small-signal device model described in section 7.2 was extended by incorporating the access resistances in series with emitter, $R_b = 10\Omega$, and collector, $R_c = 11\Omega$. The open-loop diagram is formed by a single device, and a resonator, similarly to the Fig.7.3 d). Resonator loss R_r was included as well. Simulated transfer function assuming $3mA$ bias current in the core devices is shown in the Fig.7.5.

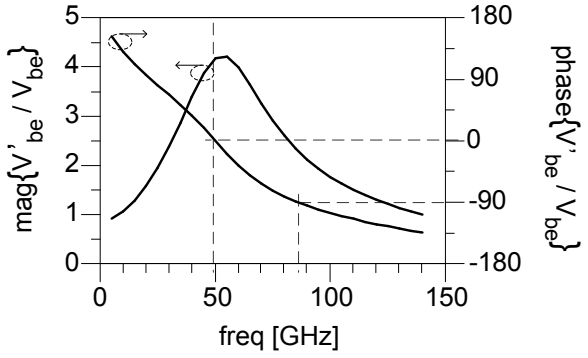

Figure 7.5: Open-loop response of the small-signal model of the simple cross-coupled oscillator.

The oscillation frequency, $f_0 \simeq 50GHz$, is where the phase response crosses zero. Magnitude of the transfer function is $\sim$4, which is sufficient for reliable oscillation startup. As expected from the simplified analysis in section 7.2.2, peak in magnitude of the transfer function is shifted up away from f_0. It was also confirmed by the simulations that the base resistance indeed had no impact on the oscillation frequency - it only flattened the phase response and degraded the gain.

Low-frequency phase response deviates strongly from what can be expected from the simple version of the equivalent circuit from the Fig.7.3. According to the eq.(7.8), the phase of that circuit converges to 90° as the frequency approaches zero. This discrepancy was found to be caused by the presence of R_e. Gain reduction due to R_e is $\sim 25\%$.

When coupled into QVCO loop, phase response of the transfer function would be further flattened, and gain and frequency would reduce due to additional loading by the coupling HBT. When R_b was halved and C_{be} doubled to account for this approximately as in the simple model before, f_0 reduced to $43GHz$ and gain became 2.2 only.

In order to tune the oscillation frequency of the QVCO, the coupling factor can be varied by changing the bias current either in the core devices T_{cr} or the coupling devices T_{cp}, as explained before. Since T_{cp} is driven 90° in advance, it can be intuitively seen that the phase characteristics in the Fig.7.5 would be shifted upwards when the oscillator is connected in a QVCO. Consequently, oscillation frequency has to increase. Therefore, if both devices inject the current, f_0 would lie between the two extremes as indicated in the Fig.7.5.

Increase of frequency can be accomplished through the increase of the bias current in T_{cp}, or decrease in T_{cr}, since both actions would increase the coupling. However, there is an additional tuning mechanism in this oscillator, namely, the C_{be} increases with current, as can be concluded from the Table 7.1. In simulation of the small-signal model, it was observed that f_0 decreased from 55 to 47 GHz when the current in T_{cr} was increased from 1 to 5 mA. If T_{cr} is used for tuning, it is easily seen that the two tuning mechanisms act in same direction. This varactor-like effect of T_{cr} would first of all expand the tuning range. But, even more important is the fact that the frequency range where the phase is steepest, and phase noise lowest, would tend to follow the oscillating frequency. On contrary, if current in T_{cp} is increased in order to increase the coupling and f_0, increase of its C_{be} would counteract that action. Therefore, tuning method by modulation of core devices provides wider useful tuning range. This was proven by harmonic balance simulations which will be described in section 7.4.1.

It was also attempted to insert a capacitance C_s in series with the base terminal. Insertion of a $11fF$ capacitor, calculated using the eq.(7.14), enhanced the oscillation frequency from 50 to 73 GHz, and increased the gain from 4 to 6. For $C_s < 9.5fF$ gain decreased very rapidly. This confirmed the usefulness of the eq.(7.14). Implementation of C_s should be seriously considered when designing the simple cross-coupled architecture in a bipolar process.

Another advantage of having C_s lies in the possibility to separate base and collector bias. In fact, transistor base in the simple oscillator in the Fig.7.2 is on same potential as collector. Applying a separate base bias would make it possible to increase the voltage swing. C_s would be especially beneficial in InP HBT based oscillators, due to large voltage swing available, and since the bipolar devices normally exhibits higher base resistance as compared to resistance of the metal gate of the field effect transistors [211]. Designs employing C_s between the transistor and the resonator circuit have been reported in various oscillator topologies, frequency bands, and technologies [117–119].

7.3 Small-Signal Approximation of the Buffered Oscillator

Another cross-coupled topology employs a pair of emitter-follower buffers T_{fb} as depicted in the Fig.7.6. A $28GHz$ QVCO based on that 'buffered' topology was demonstrated in SiGe HBT technology [49]. Variable tank capacitor was used for frequency tuning, with additional possibility to modulate the capacitances of the core HBTs. This circuit architecture is implemented in this work, but the coupling factor is used for frequency tuning. In the buffered topology the T_{fb} isolates the resonator from the parasitic loading of the other three devices, T_{cr}, T_{out}, and T_{cp} in another oscillator. This enhances the oscillation frequency and improves phase noise. The additional phase-shift of the two buffers can bring the oscillation frequency away from the tank resonance. Aim of this section is to shed a light on these issues, and to predict behavior of a QVCO based on this oscillator type.

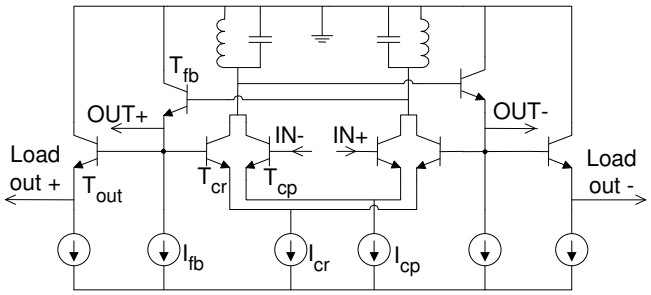

Figure 7.6: Conceptual schematic of the realized buffered oscillator topology.

7.3.1 Analysis of the Small-Signal Equivalent Circuit

Presence of the pair of feedback buffers T_{fb} in this type of oscillator significantly complicates loop analysis as well as the analysis of the tuning mechanisms in a QVCO. Simplified open-loop diagram in the Fig.7.7 (upper diagram) serves as the starting point for the discussion. The diagram was obtained following the procedure applied in the simple oscillator in the Fig.7.3: one half-part of the circuit was replaced by an ideal transformer, than the loop was opened at the base of the core transistor. The accumulated loading effect of the core-transistors T_{cr} and coupling transistors T_{cp} is described by R_{bt} and C_L as before.

The subsequent analysis process can be subdivided into two essential steps. In the first step another approximation was made, namely, C_{bc} of the core device was replaced by an equivalent capacitor $C_{bc,eq}$, across the inductor, as illustrated in the Fig.7.7 (middle diagram). In the second step, illustrated in the Fig.7.7 (lower diagram) C_{be1} of the feedback buffer was replaced by the two equivalent admittances across that device using Miller theorem. This enabled an additional break in the loop, useful for understanding this oscillator. The open-loop transfer function can than simply be viewed as a product of the two inner voltage transfer functions. The first one, V_{b1}/V_{be}, will describe the resonator on the left side. Interesting information in this part is the resonance frequency and loss which were already treated in the section 7.2.2 for various types of resonators. Possibility to have a negative conductance G_{bmi} will also reflect a risk of potential instability of the

feedback buffer within the oscillator loop. This could eventually lead to development of a parasitic oscillations or even prevent the oscillator to start-up in the wanted regime. Transfer function of the right part, V'_{be}/V_{b1}, will provide important information about departure of the oscillation frequency from the tank resonance, which is relevant for the phase-noise and choice of appropriate frequency tuning mechanism in a QVCO. The two steps will now be described in more details.

Step 1: In section 7.2 it has been shown that C_{bc} component can be replaced by two equivalent capacitors on each side of the unity gain transformer, by applying Millers theorem. Following the same idea, attempts were made to simplify this circuit in a same manner in order to separate the two voltage transfer functions - C_{bc} of $4fF$ was replaced by two complex admittances, each connected between one C_{bc} terminal and ground. The two complex admittances were tuned so to fit the two transfer functions, V_{b1}/V_{be} and V'_{be}/V_{b1}, of the two circuits from the upper and the middle diagram in the Fig.7.7. What came out of the optimization is a $C_{bc,eq} = 7fF$, which merged with C_r in the middle plot, and an another $11fF$ capacitance at the output side (not shown). The conductive parts of the two admittances were very high (in a $k\Omega$-range) and are omitted from the diagram for clarity. Using this optimized capacitance of $7fF$ it was possible to fit each of the two transfer functions with an accuracy of 5% in magnitude and 5° in phase up to $140GHz$ (around twice the resonance frequency) and in a range of bias-currents, $2 - 4mA$ for each device. The results of optimization indicate that:

- C_{bc} of the core device is again among the important contributors to the total tank capacitance.
- C_{bc}'s output equivalent of $11fF$, on contraty, does not have an important role in the total phase shift, because the output of the T_{fb} is already heavily loaded by two CE stages, as well as an output buffer stage. Therefore, the $11fF$ capacitor will be omitted from the subsequent analysis of the total phase shift, and it is omitted in the Fig.7.7. According to the simulations, this approximation will offset the phase by 5° at the tank resonance, which will not severely hamper analysis undertaken in Step 2.

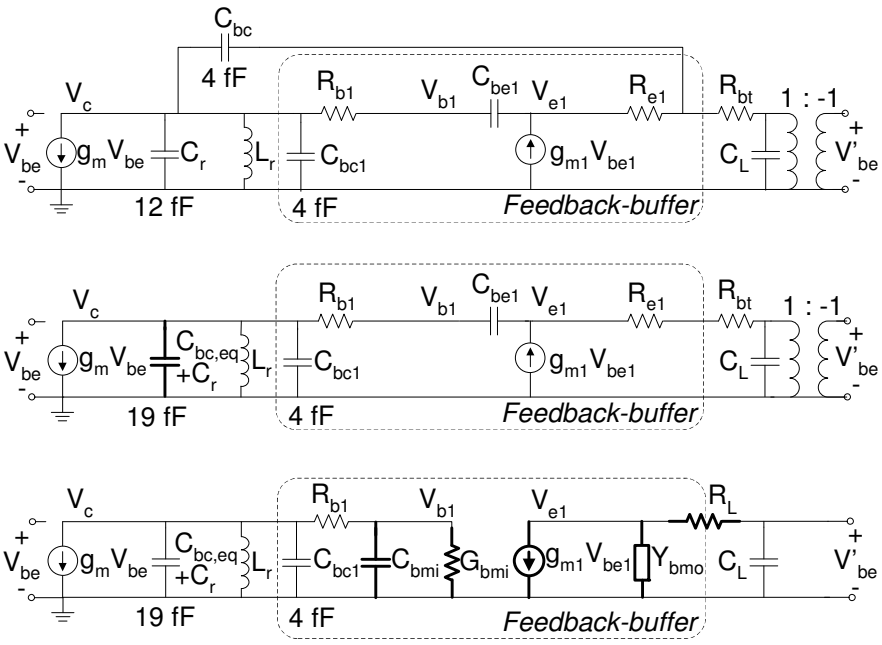

Figure 7.7: Equivalent diagram of the buffered cross-coupled oscillator. Up: Open-loop equivalent circuit. Middle: Approximative transformation of C_{bc} of the core device. Down: Miller transformation of B-E capacitance of the feedback buffer. Note that $V_{be1} = V_{b1} - V_{e1}$.

Step 2: By applying Miller theorem, as described by eq.(7.6-7.7), C_{be1}, base-emitter capacitance of the feedback-buffer was transformed into input and output equivalent admittances, as illustrated by the Fig.7.7 (lower diagram). Derivation of the following approximate expressions is presented in Appendix C. The expressions are valid in a bias and frequency range $2 - 5mA$ and $30 - 70GHz$ for a $3 \times 1.5\mu m^2$ device. Voltage transfer function used for the Miller transformation is given by

$$A = \frac{V_{e1}}{V_{b1}} \simeq \frac{g_{m1} + sC_{be1}}{\left(g_{m1} + \frac{1}{R_L}\right) + s\left(C_{be1} + \frac{C_L}{1+(\omega C_L R_L)^2}\right)}. \tag{7.15}$$

Applying A as the gain in the Miller transformation of C_{be1} to the input side, yields

$$Y_{bmi} = G_{bmi} + sC_{bmi} \tag{7.16}$$

$$\simeq \omega^2 C_{be1} \frac{\frac{C_{be1}}{R_L} - g_{m1}\frac{C_L}{1+(\omega C_L R_L)^2}}{1 + g_{m1}R_L} + sC_{be1}\frac{1}{1+g_{m1}R_L}. \tag{7.17}$$

The two calculated elements G_{bmi} and C_{bmi} are connected as shown in the Fig.7.7 (lower diagram). The conductive element becomes negative, and T_{fb} becomes potentially unstable if the following relation is satisfied:

$$\frac{g_{m1}}{C_{be1}} > \frac{1}{R_L C_L} + \omega^2 R_L C_L. \tag{7.18}$$

Both g_m and C_{be} grow linearly with a bias current of T_{fb}. However C_{be} contains a depletion capacitance term. Therefore, left part of the inequality grows with the bias current. When element values were substituted in the inequality, it was observed that G_{bmi} went negative for $I_{fb} > 3.3mA$ at 45 GHz, if the other devices were kept at $\sim 3mA$. Righthand size of this equation suggests that high value of bias current in the core device would stabilize the amplifier, because of the current dependent C_L. However, to correctly evaluate an amplifier stability, it is necessary to accurately know both real and imaginary part of the device impedance as well as the impedance seen by the device [120]. It is also necessary to have both oscillators in a QVCO. This is not possible in this simple equivalent representation of the oscillator. A more accurate method of stability check is therefore proposed and will be treated in the section 7.4.2.

The equivalent capacitance C_{bmi} from the eq.(7.16,7.17) is a downscaled version of C_{be1}, as in the case of the resistively loaded emitter-follower from eq.(7.5). The reduction factor ranges from 2 to 6.4 in a bias range of $2-5mA$ if the small-signal g_m is considered. Calculated in that way, C_{bmi} would range from 16 to 12 fF, which is 40-47% of the total tank capacitance. Since a fundamental value of a large-signal transconductance, G_{m1}, is highly dependent on a drive level of a bipolar device [161], its value will in general be different from g_m. Therefore, the actual C_{bmi} would depend on the signal level as well.

Consequently, oscillating frequency and quality factor would be dependent on the nonlinear effects and difficult to predict. Recall that a small C_{bmi} is desired since this capacitor is charged through R_b. The buffered oscillator therefore offers the possibility to realize higher quality resonator as compared to the simple oscillator case, where the resonator was directly loaded by the two CE stages and the output emitter-follower.

Miller transformation of C_{be1} to the output side determined Y_{bmo} component from Fig.7.7 (lower diagram). After that, a close approximation to the angle of the voltage transfer function $V_{be}^{'}/V_{b1}$ was found,

$$\angle\left(\frac{V_{be}^{'}}{V_{b1}}\right) \simeq -\arctan\left(\frac{1+g_{m1}R_L}{\frac{\omega C_{be1}}{g_{m1}}+\frac{g_{m1}}{\omega C_L}}\right). \tag{7.19}$$

The derivation details can be found in the Appendix C. Apparently, the angle lies between $0°$ and $-90°$, which means that the free-running oscillator will operate below the tank resonance frequency. After substitution of the small-signal element values for the two devices biased at $3mA$, the phase offset calculated at 55 GHz became $-58°$. As in the eq.(7.17), the drive dependent transconductance G_{m1} should be used in stead of small-signal g_{m1}, making it difficult to predict the phase-shift in the steady-state regime.

7.3.2 Simulated Open-Loop Response

Simulation of the open-loop voltage transfer characteristics of the single buffered oscillator, is performed using small-signal models of the core and feedback device, extracted at $3mA$ as in the case of simple oscillator in section 7.2.3. To improve the accuracy of the models, access resistances of 10 and 11 Ω in emitter and collector, respectively, were introduced. The oscillator loop was composed of two device models, representing the core and feedback device, respectively, and resonator with parasitics. The obtained transfer function is plotted in Fig.7.8.

Phase curve crosses zero at around $65°$ above the point where the peak in magnitude occurs, which is in reasonable agreement with a simplified analysis above, where $58°$ was predicted.

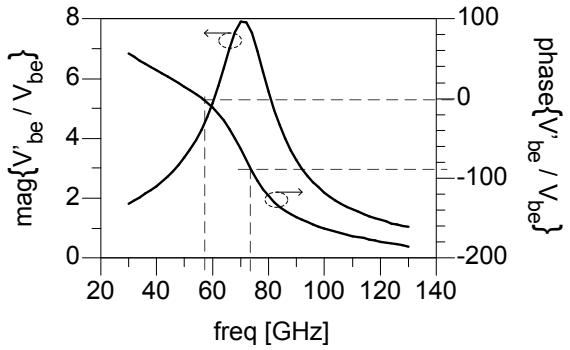

Figure 7.8: Open-loop response of the small-signal model of the buffered oscillator.

If two oscillators were coupled in a QVCO, the phase shift would become even more negative, because of the additional capacitive loading by the coupling device on the output of the feedback buffer. When R_b was halved and C_{be} doubled to approximately account for this, an additional phase shift of -12° was observed. This again created a $5GHz$ negative offset in frequency. Gain at the oscillation frequency reduced from 4.6 to 2.9.

Oscillation frequency of a QVCO based on the buffered oscillator would increase with the coupling, as it was the case with the QVCO based on the simple oscillator. Similarly, increase of the coupling can either be accomplished through the increase in the current in the coupling devices, or decrease in the current in the core devices. What is different from the simple oscillator case is that this frequency shift would bring the oscillator *towards* the tank resonance frequency. Accordingly, phase noise would *improve* with increasing the coupling factor and the oscillation frequency.

7.4 QVCO Simulations Using Nonlinear HBT Model

In this section, the simple and the buffered oscillator topologies will be further evaluated as building blocks of a QVCO. The discussion is based on various simulations performed in ADS.

7.4.1 Harmonic Balance Simulation of the Two QVCO versions

Performance of the two QVCOs based on the simple and buffered oscillator topologies, here denoted as QVCO1 and QVCO2, respectively, were compared using Harmonic Balance (HB) simulation. Circuit diagrams of the two topologies have been presented in Fig.7.2 and Fig.7.6, respectively. Coupling devices of the QVCOs were biased at 2.5 mA. All the output buffers as well as the feedback buffer of the QVCO2 were biased at $4.1mA$ for high gain. Diode-connected core and coupling devices of the QVCO1 are limited to V_{ce} bias voltage range of $0.7 - 0.85V$, while those of the QVCO2 are limited to roughly double that voltage. This is an inherent advantage of the buffered topology, since larger voltage swing can be developed across the devices. Simulation results are presented in Fig.7.9.

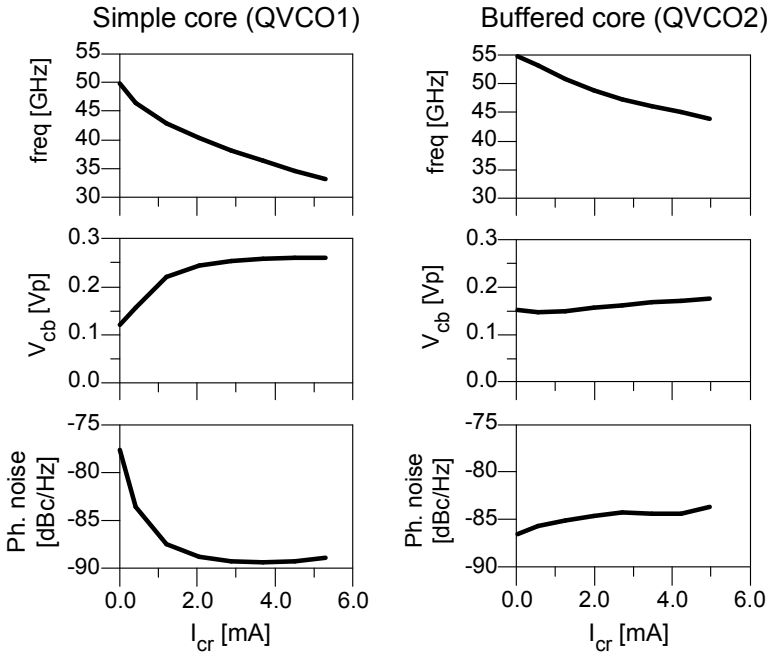

Figure 7.9: HB simulation results for the two investigated QVCO versions. Oscillation frequency, base peak voltage driving the output HBTs and phase-noise at 1-MHz offset from the carrier, plotted versus DC-current in the core transistors.

The oscillation frequency of both QVCOs increases with decreasing bias current I_{cr} in the core devices, as expected. The voltage swing V_{cb}, and hence the output power, of the QVCO1 rapidly decays as I_{cr} is reduced below 2 mA. One mechanism responsible for this phenomenon is the dependence of device gain on I_{cr}. Another reason is that the magnitude of the loop transfer function reduces as the frequency increases above the tank resonance. Likewise, the phase noise increases rapidly due to this sudden decrease in V_{cb} and due to flattening of the phase characteristics away from the resonance.

Recall that the loop transfer function of the simple oscillator peaks slightly above the oscillation frequency. Furthermore, the bias modulated C_{be} supports the tuning mechanism by moving the resonance frequency in the same direction. These two effects in the QVCO1 are responsible for the almost constant phase noise and voltage in a relatively wide frequency range.

Dependence of the transfer function magnitude on I_{cr} seems to be more favorable in QVCO2 case. As I_{cr} and device gain is reduced, the frequency is shifted *towards* resonance, where the magnitude of the transfer function is higher. This is reflected in the relatively constant voltage swing as compared to the QVCO1 case. The phase noise performance improves near resonance, as expected. This improvement is also supported by the fact that the core devices inject less noise at reduced I_{cr}.

Tuning range of both QVCOs was roughly 50% lower when coupling transistors were used for tuning. The phenomenon has been explained before by the bias dependence of C_{be} in QVCO1. The tuning mechanisms are more complicated in the QVCO2 case. One possible explanation is that the bias dependent C_{be} of the core and coupling devices controls the phase-shift through the eq.(7.19).

Frequency tuning of the two single oscillators was simulated as well. By changing the currents from 2 to 4 mA, the simple and the buffered oscillators were tuned in frequency ranges of 39-46 GHz and 48-54 GHz, respectively. The output buffers were removed as in the small-signal simulations. It turns out that center frequencies of the two bands lie around 8 and 7 GHz, respectively, below the frequencies predicted by the small-signal models. This discrepancy is believed to

be partly caused by the small-signal approximation of the transistor in the analytical formulation.

In a wide frequency range the QVCO1 exhibits significantly lower phase noise as compared to QVCO2. This is partially due to the fact that the QVCO2 operates at roughly 25% higher frequency. This corresponds to a $1.9dB$ degradation in phase-noise as it can be expected from Leeson's equation (3.2). Moreover, feedback-buffers contribute $\sim 2dB$ to the phase-noise power. Despite that, when a $44fF$ capacitor is added across the resonator inductor in the QVCO2, in order to shift it to lower frequency range of QVCO1 where the Q-factor was higher, it surpassed the QVCO1 by at least 1.3 dB in the achieved tuning range, 36.5-42 GHz. This tuning range is comparable to that achieved by the QVCO1 before the onset of strong phase-noise degradation, as suggested by the Fig.7.9. The near-resonance operation is especially more attractive in the QVCO2 architecture, since high-frequency and low-noise performance are combined. After addition of the 44 fF capacitance in the QVCO2 tank, the tuning range shrank from 20% to 14%, since the phase of the tank impedance became steeper, and also because the modulated device capacitances constituted smaller part of the total capacitance.

7.4.2 Simulations of the Implemented QVCO

Circuit diagram of one oscillator of the implemented QVCO is shown in Fig.7.10. The $2\times115pH$ planar inductor was implemented as a single turn, with grounded center tap, and it was EM simulated in Momentum software. The HBT bias currents were presented in section 7.4.1. The frequency is tuned by V_{tune} voltage, which determines the current through the core devices T_{cr}. The current source T_t with a large emitter length, L_E=$20\mu m$, was employed to postpone saturation of that device to high current, $9.5mA$. Aiming at high oscillation frequency, smallest emitter size, $3\mu m$, is chosen for all other devices, which minimized the parasitic capacitances in the core. Though larger emitter lengths, 6 and $10\mu m$, exhibit slightly higher f_t and f_{max} [133, 135], oscillation frequencies achievable using these HBTs were, respectively, 5 and 7 GHz lower, owing to their larger capacitances. The intercon-

nects were modeled using ADS microstrip model MLIN. The simulation results are presented in Fig.7.11.

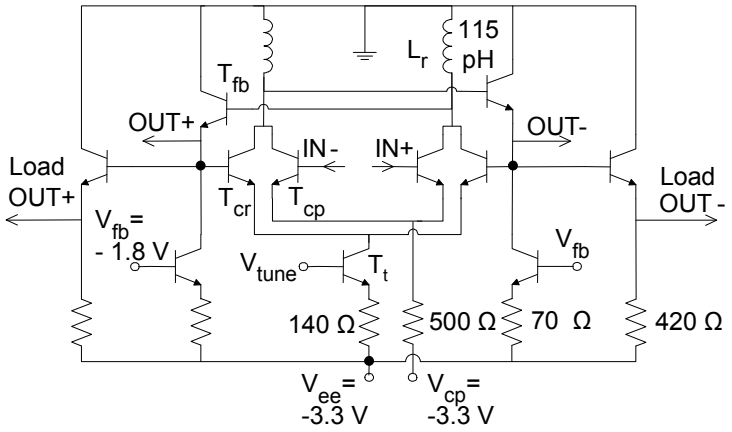

Figure 7.10: Circuit diagram of the implemented buffered type oscillator of the QVCO.

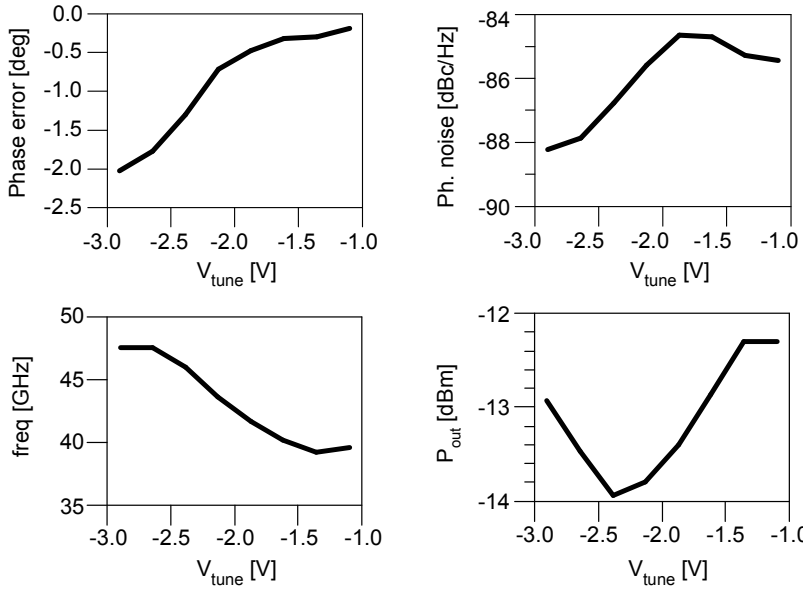

Figure 7.11: Simulated phase error, phase noise, frequency and single-ended output power of the implemented QVCO. The data are plotted versus tuning voltage swept from -2.9 to -1.1 V in 0.3 V steps.

Due to the inductive behavior of the interconnecting lines, the circuit now oscillates around 8 GHz below the oscillation frequency of the interconnect-free QVCO2, which performances have been presented in the Fig.7.9. The phase-noise curve did not changed substantially. The oscillator is tuneable between 39.5 and 47.5 GHz. Reducing the inductor value from 115 to 90 pH would result in higher oscillation frequency, 52.5 GHz. The price for this frequency enhancement would be around 4 dB higher phase-noise and 2 dB lower output power.

Phase error in the Fig.7.11 is calculated as a deviations from the 90°-phase relationship between two single ended QVCO outputs. The phase error results from imperfections in the layout symmetry. The error is increasing with frequency. As the frequency approaches the tank resonance phase noise improves and phase error increases. This is in agreement with theoretical studies on this subject [209,212]. However, as pointed out before, behavior of this QVCO deviates from these theoretical models, in the sense that the oscillation frequency *approaches* the resonance frequency as the coupling gets stronger.

Stability of the Feedback Buffer

Simplified analysis of the buffered cross-coupled oscillator presented in the section 7.3 predicted a risk of parasitic oscillations in the oscillator loop, arising from a possibility to have negative resistance seen into the base of the feedback buffer. In order to have more accurate results, the full QVCO simulation setup described in the section 7.4.2 was employed. In the proposed small-signal simulation the loop was broken at the base of the feedback device T_{fb} in a single oscillator of the QVCO. The resulting two open ends, one looking into the base, and another towards the other direction are denoted as A and B, respectively, in the Fig.7.12. In order to simulate the correct impedance seen into terminal A, the terminal B has to see the impedance of the terminal A. This was accomplished by employing another open-loop QVCO, which served as a termination to the first one. Continuing so, a chain of QVCOs is formed as depicted. It was found by experimenting that five QVCOs should be sufficient in order to make Z_A insensitive to the impedance seen by the other end, and vice versa.

Now Z_A and Z_B represent the correct impedance values seen into the open terminals of a QVCO. Two conditions for the oscillation startup in a negative-resistance oscillator are [120]

$$R_A + R_B < 0, \qquad X_A + X_B = 0 \tag{7.20}$$

where $R_{A,B}$ are real and $X_{A,B}$ are imaginary parts of the two impedances seen from the reference plains where the loop is open. In other words, an oscillation in a system would start up at a frequency where the two reactances cancel, and the sum of the two real parts is negative. To verify whether the two conditions are satisfied in the QVCO, Z_A and Z_B are simulated and plugged into the eq.(7.20). Result for the QVCO biased at $V_{tune} = 2V$ is shown in the Fig.7.13 (left plot).

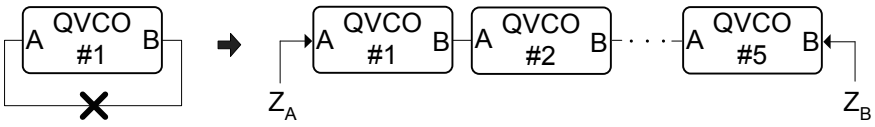

Figure 7.12: Small-signal stability simulation setup with cascaded QVCO's. Each QVCO loop is broken at same node.

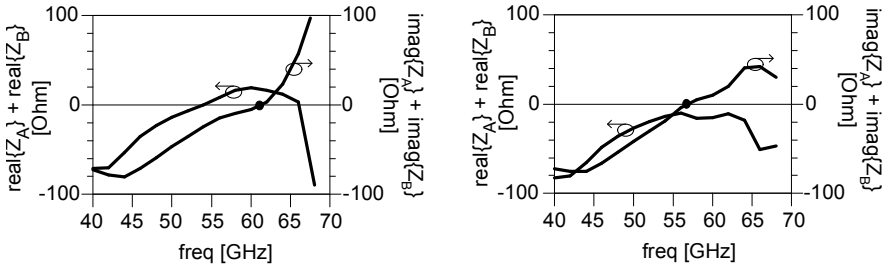

Figure 7.13: Simulation results for the setup from the Fig.7.12, before (left plot) and after (right plot) insertion of a $30pH$ inductor in series with collector of T_{fb}.

Fortunately, $(R_A + R_b)$ is positive where $(X_A + X_B)$ crosses zero, around 62 GHz. It was found that decreasing the bias current in T_{fb} from $4.1mA$ to $1mA$ had a beneficial impact on the circuit stability,

through the increase of R_A by 7Ω. This trend can be expected from the approximative equation (7.18).

Attempts were also made to identify the elements in the circuit which would make the QVCO unstable. It turned out that the circuit stability is rather dependent on parasitic inductance in series with the collector of T_{fb}. Inserting a $30pH$ inductor in that path makes the circuit unstable at 57 GHz, as depicted in Fig.7.13 (right plot). This parasitic oscillation mode of the modified circuit was also verified in HB simulator. The QVCO oscillated around 54 GHz, but the signals were not in quadrature. Phase relationships between the output signals were highly disordered and dependent on the actual bias conditions.

7.5 Experimental Results

A photograph of the realized QVCO, is provided in the Fig.7.14. Aiming at high oscillation frequency, special care was devoted to design the oscillator core with short interconnects. A thinnest allowable line width of 4 μm was used for the interconnects, which reduced the core area, and thereby the length of these lines, as well as the parasitic capacitances. Characteristic impedance of the 4 μm microstrip line is $\sim 120\Omega$ and the longest line is $75\mu m$ long. At $45GHz$ quarter wavelength is $\sim 640\mu m$. Hence the lines have predominately inductive behavior. For the sake of quadrature accuracy, the overall layout was organized with a high degree of symmetry.

Fig.7.15 illustrates the setup for measurement of the oscillation frequency and the output power. The two oscillators of the QVCO, referred as OSC1 and OSC2, respectively, are connected to the power supplies through the PPPP power probes, and to the Agilent E4448A spectrum analyzer through the Cascade Microtech ACP40-D double-tip GSGSG probes. Supply voltages V_{ee} and V_{cp} are connected to -3.3V, and V_{fb} was used to adjust the current through the feedback devices. Frequency tuning is carried out through variation of V_{tune}. Single-ended output powers were recorded one by one for each output, while tho other three outputs were terminated by 50Ω terminations. Power losses in the cables, DC-blocks and probe heads were estimated

using a through calibration standard, and subtracted from the measurements. It was unfortunately not possible to measure quadrature accuracy and phase noise using the available equipment.

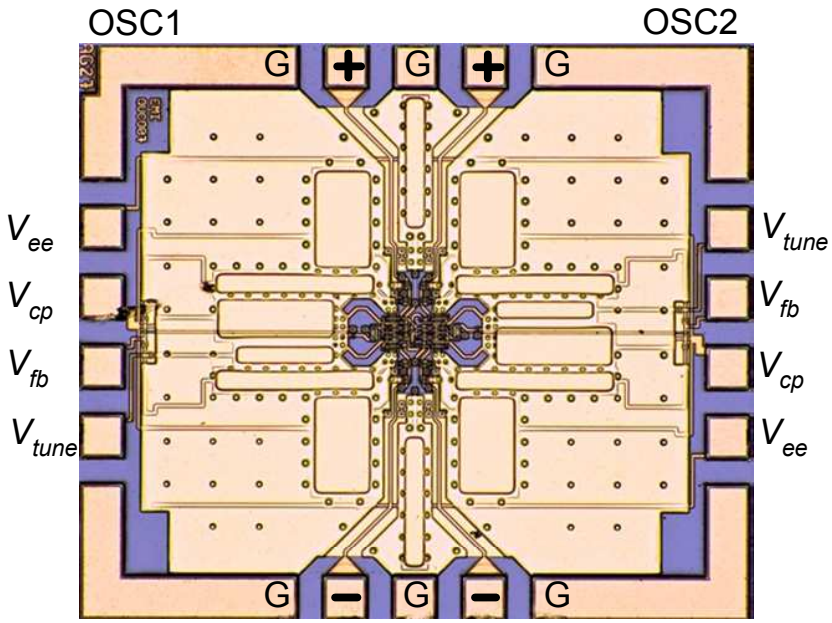

Figure 7.14: Photograph of the $1.45 \times 1.25\ mm^2$ QVCO die.

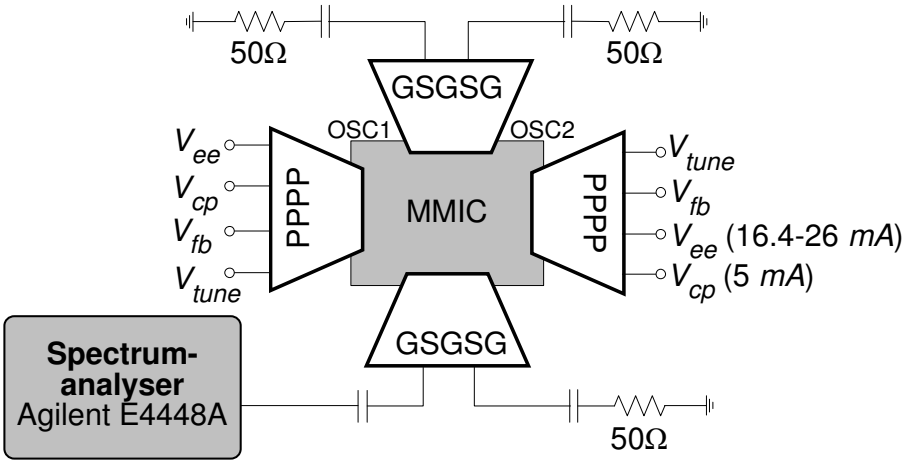

Figure 7.15: Measurement setup.

The measured power and frequency versus tuning voltage are presented in the Fig.7.16. Output power P(OSC1) was calculated as an average power of the two single ended outputs of the oscillator OSC1. The presented P(OSC2) is calculated in the same way for the OSC2. It is believed that the deviation between the two power-curves is caused mainly by asymmetry in the setup, e.g. with respect to bias currents and losses in the cables and the bias tees. Power variation across the tuning range is low, as can be expected from the simulations.

Single-ended power averaged across whole tuning range is 14.7 dBm. This is about $1.5dB$ lower than expected from the simulated results in the Fig.7.11. The achieved tuning range is $3GHz$ wider than expected - the lowest operating frequency is downshifted by 2.5 GHz, and the highest frequency is upshifted by 0.5 GHz. Power level in the circuit is sensitive to the series base resistance R_b forming a voltage divider with C_{be} in the core devices. Tuning range is also sensitive to it since R_b flattens the phase characteristic of the resonator. An attempt to increase R_{bi} parameter in the HBT model from 44 to 60 Ω caused both the power and the tuning range to agree with simulations.

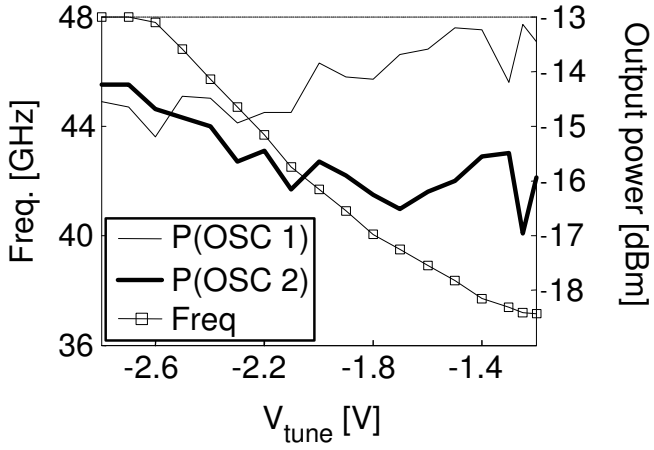

Figure 7.16: Measured frequency and output power of the two oscillators of the QVCO.

Table 7.2, which compares the developed QVCO to the other high-frequency QVCO MMICs. The achieved oscillation frequency and tuning range represent state-of-the-art results.

Technology	Tuning range $[GHz]$	Phase noise @1(3) MHz $[dBc/Hz]$	P_{out} $[dBm]$	Ref.
90nm SOI CMOS	38-43	(-80...-87)	>-7.5	[45]
90nm CMOS	31-41	-104*		[46]
0.25μm BiCMOS (CMOS)	23-24.4	-94		[47]
0.25μm BiCMOS (SiGe HBT)	30.6-32.6	-97		[48]
0.4μm SiGe HBT	24.8-28.9	-84.2	-14.7**	[49]
1.5μm InP HBT	37-47.8	-85...-88* (-95...-98*)	-14.7	this work

* simulated, **per differential output

Table 7.2: Published QVCOs and this work.

7.6 Discussion

Number of assumptions were made while analyzing the simple and the buffered cross-coupled oscillators using a feedback approach. In spite of that, the equivalent circuits provided a useful insight into the oscillator behavior. The analysis identified series base resistance, B-E capacitance and interconnect line inductance as the major performance limiting factors in a differential oscillator. Moreover, if a high oscillation frequency is desirable, interconnecting lines should be routed such that largest parasitic capacitances in a loop concentrate around the resonator inductor. The analysis also encompassed the series resonator capacitance that can be used to extend the operating frequency and loop gain. A simple analytical expression for optimum capacitance value was suggested.

The QVCO architecture based on the buffered oscillator type behaves fundamentally different from that based on the simple differential oscillator - as the coupling strength increases, the oscillation frequency approaches the tank resonance frequency. A stand-alone buffered oscillator would operate below the resonance where the phase noise is relatively high. However, when the frequency is shifted up by a strong coupling in a QVCO, it offers an improved phase-noise and

high frequency simultaneously. At the highest simulated frequency of 47.5 GHz, phase noise is -88 dBc/Hz. Modulation of the device capacitances interacts with the coupling control mechanism, and can be exploited to increase the useful tuning range without compromising the phase noise.

A straightforward linear simulation method for detecting unwanted oscillation modes in a QVCO was suggested and applied to the buffered QVCO architecture.

A first InP HBT based QVCO for mm-wave frequency range was developed. It was based on the buffered oscillator type. The circuit generated an average power of -14.7 dBm per single-ended output, and exhibited state-of-the-art frequency of operation and tuning range, 37-47.8 GHz. These results are in reasonable agreement with the simulations. Simulated phase noise ranged from -85 to -88 dBc/Hz at $1MHz$ offset from the carrier. The presented results prove the suitability of InP HBT process from ATL for implementation of mm-wave quadrature oscillators.

Chapter 8

Conclusions and Future Work

Conclusions

Throughout this thesis, a technology investigation and design of circuits for signal generation and amplification has been performed in view of efficiency, power and frequency of operation. For construction of circuits it has been aimed at high-breakdown technologies. Gallium-nitride HEMT technology was used to deign a microwave high-power amplifier, while indium-phosphide HBT technology was selected for the design of mm-wave power amplifier and quadrature VCO.

One-tone measurements of the investigated GaN HEMT device, performed at 8 GHz, indicated that deep class-AB bias provides a good balance between high gain and power added efficiency. In a two-tone test, same bias point offered lowest third order intermodulation distortion (IMD3) at power levels beyond $1dB$ back-off. An IMD3 better than -30 dBc was measured at output powers ranging up to $2dB$ compression level. The design of two-stage $8GHz$ PA MMIC was accomplished based on power HEMTs biased in deep class-AB (80 mA/mm). Regarding the PAE enhancement at this operating point, a 2^{nd} harmonic tuning turned out to be an essential design issue, and was applied to the output-stage transistors. Simulated source and load 2^{nd} harmonic impedances, needed for highest PAE, resulted in voltage and

current waveforms that resemble those of a parallel-tuned amplifier with short-circuited harmonics. Without accounting the undertaken harmonic manipulation and associated PAE enhancement, a PAE of 31.3% and 42.5 dBm saturated output power are expected from the PA circuit. These results are competitive to those reported for the state-of-the-art MMICs. The simulated small-signal gain is $21dB$, and $1dB$ bandwidth is from 7.7 to 8.4 GHz. The PA would hence be useful in satellite uplink communications. The circuit is being fabricated.

At millimeter-wave frequencies InP HBT technology offers attractively high bias voltage and power density. This inspired investigation of InP HBT technology for the E-band PA design. High power density is, however, also offered by SiGe HBTs. To get a deeper insight into the characteristics of the two HBT technologies, an accurate small-signal and large-signal VBIC model of a $0.21\mu m$ SiGe HBT have been extracted. For this purpose, a widely used 'open-short' de-embedding method was improved to account for distribution of the HBT test structure parasitics. A method to correct a de-embedding error resulting from probe positioning inaccuracy was also suggested.

When simulated in a $73GHz$ power amplifier, the SiGe HBT device shows seven times higher DC-current per unit emitter area as compared to the provided InP HBT device. Despite that fact, the SiGe HBT shows lowest junction temperature. High breakdown voltage of the InP HBT facilitates, however, higher output power, efficiency and the design of matching circuits. Regarding the second-order effects in the investigated HBT devices, large oxide capacitance severely reduces input and output impedances of the SiGe HBT, while high collector resistance diminishes the output power of the InP HBT.

A two-stage InP HBT power amplifier employing $8\times(10\times1.5\ \mu m^2)$ device periphery in each stage has been developed. The driver stage saturates at high power levels and improves linear performance. The developed four-transistor power cell provides equal combining characteristics and load impedance to all four HBTs. Resistors integrated with the bias circuitry assured stability of the PA stages, without compromising the gain. A method for simulating odd-mode oscillations has been presented and successfully applied to stabilize the driver stage using a single resistor. The PA demonstrated peak small-

signal gain of 7.5 dB at 77 GHz while drawing 320 mA from a 2.4V supply. The 3dB gain bandwidth was 45%. The simulated output power, ∼150 mW with PAE of 15% are record results for an InP HBT PA operating above 50 GHz. Deviations between simulated and measured S-parameters will eventually cause degradations in the predicted output power and PAE.

Another circuit developed in InP HBT technology is a mm-wave quadrature VCO. This is, to the author's knowledge, the only InP HBT based mm-wave QVCO reported to date. Together with the developed InP HBT PA, this oscillator has potential application in E-band communication front-end. The frequency is tuneable through variation of the coupling strength between the two identical LC-oscillators. Modulation of the bias-dependent HBT capacitances interacts with the coupling control mechanism, and was exploited to increase the QVCO's tuning range without compromising its phase-noise. Two differential cross-coupled oscillator topologies were analyzed using feedback approach. It was shown that the $C_{be}R_b$ time constant is among the most important performance limiting factors in the HBT. Achievement of a high oscillation frequency demands that, the interconnects are routed such that the largest capacitances in the loop concentrate around the parallel resonator inductor. A resonator coupling capacitor can be used to extend the operating frequency and loop gain, and an expression for the optimum capacitance value was suggested. A simple linear simulation method for detecting unwanted parasitic oscillations in a QVCO was presented and applied to the developed QVCO. The MMIC generated an average power of -14.7 dBm per single-ended output, and exhibited state-of-the-art frequency and tuning range, 37-47.8 GHz. These data were in reasonable agreement with the simulations. Simulated phase noise ranged from -85 to -88 dBc/Hz at 1MHz offset from the carrier.

Future Work

Circuit analysis and designs undertaken in this thesis dealt with some important issues within the field of signal power generation and amplification at microwave and mm-wave frequencies. Nevertheless, there are still plenty of challenges to be met.

Availability of accurate GaN HEMT models will aid in the development of highly linear and highly efficient high-power amplifiers. In particular, optimization of two-stage solutions will benefit from better model accuracy. Moreover, power amplifier optimization at higher power levels, e.g. in light compression regime, will be possible.

The first attempts to develop a high power amplifier and a high-frequency QVCO in the used InP HBT process brought some promising results. The next InP HBT MMIC to be designed for the 71-86GHz E-band transmitter chipset will be a subharmonic mixer. Future activities will moreover seek to enhance the amplifier gain and oscillator phase-noise performance, through assessment of other circuit architectures. The acquired knowledge will eventually push the circuit design towards higher power levels and higher frequencies.

Appendix A

GaN HEMT Power Amplifier Schematic

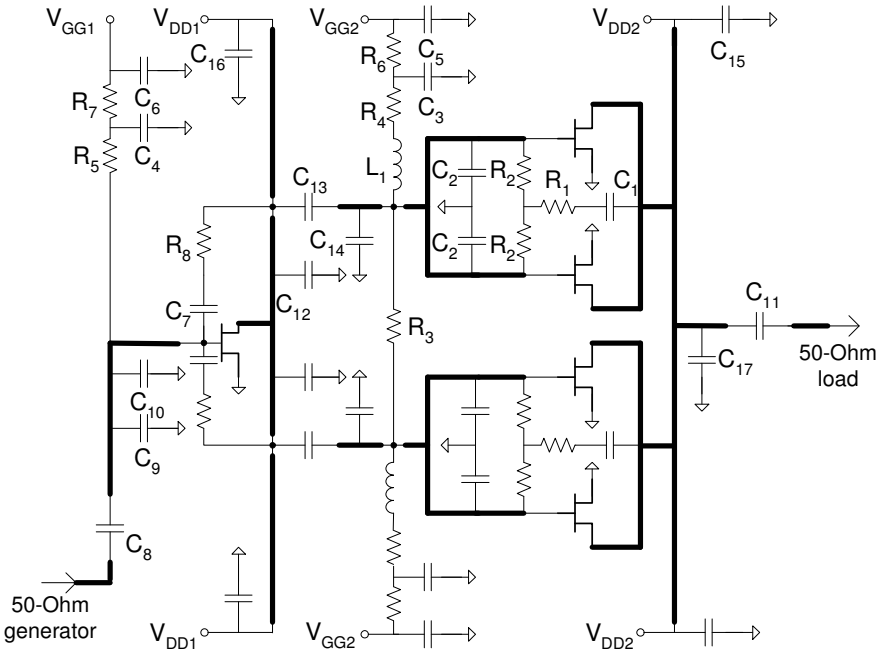

Figure A.1: Circuit diagram of the realized power amplifier. Component values are identical in the two circuit half-parts symmetrical around horizontal center axis.

Component	*Value*	*Unit*	*Component*	*Value*	*Unit*
L_1	627	pH	C_4	38	pF
R_1	190	Ω	C_5	15.5	pF
R_2	10	Ω	C_6	50	pF
R_3	10	Ω	C_7	900	fF
R_4	6.67	Ω	C_8	1763	fF
R_5	15	Ω	C_9	876	fF
R_6	30	Ω	C_{10}	876	fF
R_7	5	Ω	C_{11}	1800	fF
R_8	150	Ω	C_{12}	1187	fF
C_1	1800	fF	C_{13}	1066	fF
C_2	590	fF	C_{14}	1018	fF
C_3	5	pF	C_{15}	20	pF
			C_{16}	20	pF
			C_{17}	1475	fF

Table A.1: Component values for the PA circuit from the Fig.A.1.

Appendix B

InP HBT Power Amplifier Schematic

Component	*Value*	*Unit*	*Component*	*Value*	*Unit*
C_{s1}	192	fF	C_{c2}	1.17	pF
C_{s2}	209	fF	C_{c3}	11.4	pF
C_{s3}	270	fF	C_{c4}	1.14	pF
C_{p1}	279	fF	L_{b1}	286	pH
C_{p2}	322	fF	L_{b2}	286	pH
C_{b1}	362	fF	R_{b1}	80	Ω
C_{b2}	1.6	pF	R_{b2}	80	Ω
C_{b3}	176	fF	R_{c1}	15	Ω
C_{b4}	2.21	pF	R_{c2}	15	Ω
C_{c1}	15.7	pF	R_{odd}	10	Ω

Table B.1: Component values for the PA circuit from Fig.B.1.

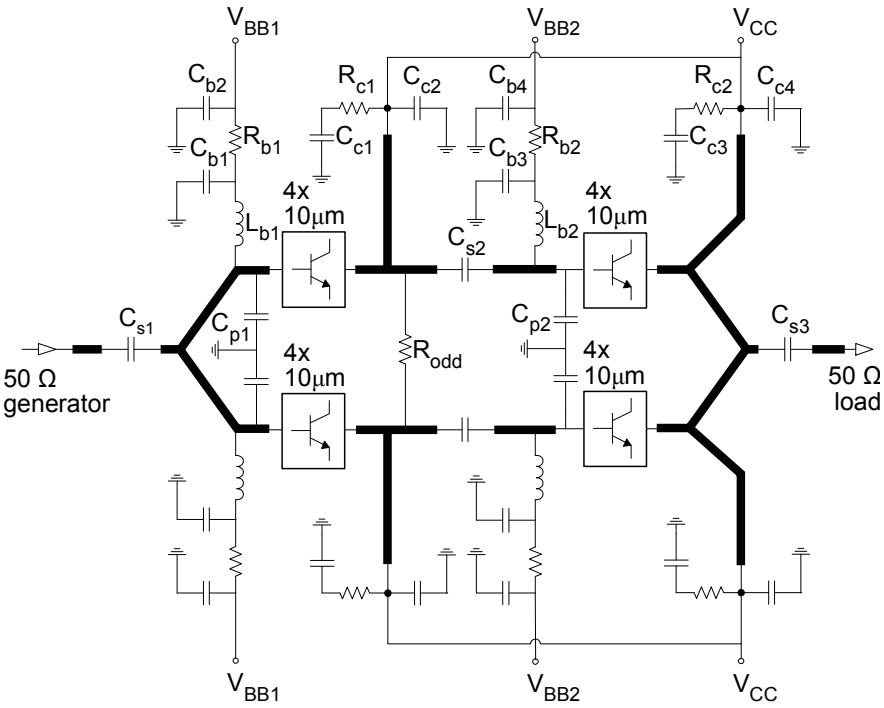

Figure B.1: Schematic for the developed InP HBT power amplifier MMIC. The MIM capacitors C_{p1} and C_{p2} are incorporated into the power cells as indicated in the cell layout in Fig.6.3.

Appendix C

Derivations of the Oscillator Equations

This appendix explains the derivation of the equations for the simplified small-signal oscillator model from the Fig.7.7 (lower plot). The diagram is repeated in the Fig.C.1.

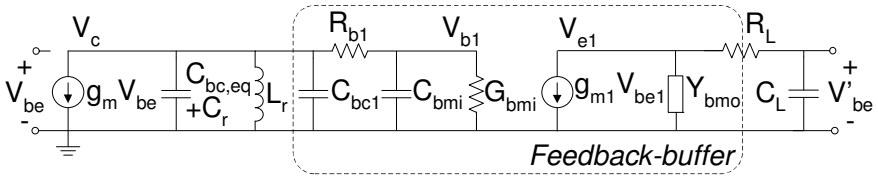

Figure C.1: Simplified equivalent diagram of the buffered cross-coupled oscillator. A copy of the Fig.7.7 (lower plot).

All approximations in the following analysis were validated in frequency range 30-70GHz, and 2-5mA bias currents I_{fb} and I_{cr} of the feedback buffer and core transistors, respectively. Note that I_{cr} in the simplified small-signal model represents the current of three different devices, core, coupling and output device, but in the real circuit, only the core device current is varied. To reduce the size of the expressions in the following derivations, a frequency dependent subfunction F is introduced,

$$F = \frac{1}{1 + (\omega C_L R_L)^2}. \tag{C.1}$$

Here, the product $C_L R_L$ is the time constant of the parasitics loading the feedback-buffer. The cut-off frequency $1/(2\pi C_L R_L)$ ranges from 24 to 37 GHz in the given bias-current range of the loading-transistors.

Voltage transfer function V_{e1}/V_{b1} of the buffered oscillator small-signal equivalent circuit from the Fig.C.1 is found to be

$$A = \frac{V_{e1}}{V_{b1}} = \frac{g_{m1} + sC_{be1}}{\left(g_{m1} + \frac{1}{R_L} - \frac{F}{R_L}\right) + s\left(C_{be1} + C_L F\right)} \tag{C.2}$$

$$\simeq \frac{g_{m1} + sC_{be1}}{\left(g_{m1} + \frac{1}{R_L}\right) + s\left(C_{be1} + C_L \frac{1}{1+(\omega C_L R_L)^2}\right)} \tag{C.3}$$

The F/R_L is neglected in the eq. C.3 since it is at least 6.7 times smaller as compared to the sum of the other real terms. The expression is increasingly valid as the frequency goes beyond 30 GHz, since the F-term disappears.

Miller transformation of the C_{be1} to the input side of the feedback-buffer provides the equivalent input admittance

$$Y_{bmi} = sC_{be1}(1 - A) \tag{C.4}$$

$$= sC_{be1} \frac{\left(\frac{g_{m1}}{R_L} + \frac{1}{R_L^2}\right) + \omega^2 C_L F\left(C_{be1} + C_L F\right) + s\left(g_{m1} C_L F - \frac{C_{be1}}{R_L}\right)}{\left(g_{m1} + \frac{1}{R_L}\right)^2 + \omega^2\left(C_{be1} + C_L F\right)^2} \tag{C.5}$$

$$\simeq \omega^2 C_{be1} \frac{\frac{C_{be1}}{R_L} - g_{m1}\frac{C_L}{1+(\omega C_L R_L)^2}}{(1 + g_{m1} R_L)} + sC_{be1}\frac{1}{1 + g_{m1} R_L} \tag{C.6}$$

$$= G_{bmi} + sC_{bmi}. \tag{C.7}$$

Two simplifications have been made in eq.(C.5). Namely, the ω^2-terms in numerator and denominator have been neglected since they are more than order of magnitude smaller than the two other real terms in the numerator and the denominator, respectively. Y_{bmi} component will affect behavior of the resonator in the Fig.C.1.

Similarly, an equivalent impedance

$$Y_{bmo} = sC_{be1}\frac{1}{1-A} \tag{C.8}$$

$$= sC_{be1}\frac{\frac{-1}{R_L} - sC_LF}{g_{m1} + sC_{be1}} \tag{C.9}$$

$$= sC_{be1}\left[-\frac{\omega^2 C_{be1}C_LF - \frac{g_{m1}}{R_L} + s\left(\frac{C_{be1}}{R_L} - g_{m1}C_LF\right)}{(\omega C_{be1})^2 + g_{m1}^2}\right] \tag{C.10}$$

$$\simeq \frac{\omega^2 C_{be1}}{g_{m1}}\left(C_LF - \frac{C_{be1}}{g_{m1}R_L}\right) - s\frac{C_{be1}}{g_{m1}R_L} \tag{C.11}$$

can be connected to the output side. It was shown that the two ω^2-terms in eq.(C.10) are more than order of magnitude smaller as compared to the dominant real terms in the numerator and denominator, respectively. Therefore they have been omitted in the derivation of the eq.(C.11).

The two admittances of the Miller equivalent circuit from the Fig.C.1 are now derived. Next step towards determination of the oscillation frequency is to find the voltage transfer function $V_{be}^{'}/V_{b1}$. It is given by

$$\frac{V_{be}^{'}}{V_{b1}} = \frac{g_{m1}}{(sC_LR_L+1)\left(Y_{bmo} + \frac{1}{R_L} + g_{m1}\right) - \frac{1}{R_L}} \tag{C.12}$$

$$\simeq \frac{g_{m1}}{(sC_LR_L+1)\left(-s\frac{C_{be1}}{g_{m1}R_L} + \frac{1}{R_L} + g_{m1}\right) - \frac{1}{R_L}}. \tag{C.13}$$

where the approximation is justified by the fact that the real part of the Y_{bmo} from the equations (C.8)-(C.11) is two orders of magnitude smaller as compared to $1/R_L+g_{m1}$. Separation of the Y_{bmo} in eq.(C.11) into real and imaginary part has greatly simplified the subsequent derivations, since its rather large expression is reduced to a single imaginary term. Expression for the angle of the transfer function from eq.(C.13) becomes relatively simple,

$$\angle\left(\frac{V_{be}^{'}}{V_{b1}}\right) = -\arctan\left(\frac{1+g_{m1}R_L-\frac{C_{be1}}{C_L g_{m1}R_L}}{\frac{\omega C_{be1}}{g_{m1}}+\frac{g_{m1}}{\omega C_L}}\right) \tag{C.14}$$

$$\simeq -\arctan\left(\frac{1+g_{m1}R_L}{\frac{\omega C_{be1}}{g_{m1}}+\frac{g_{m1}}{\omega C_L}}\right). \tag{C.15}$$

The neglected last term of the numerator of eq.(C.11) is more than 20 times smaller than $(1 + R_L g_{m1})$ in above-mentioned frequency range and bias range. Figure C.2 compares the calculated phase of eq.(C.15) with with an exact phase, calculated without any simplifications made in this chapter. Despite of the simplifications, an excellent agreement has been achieved in the expected bias range, 2-5 mA and frequency range 30-70 GHz. At lower bias of the feedback buffer, $I_{fb} < 2mA$, the equation C.15 is not longer valid in the higher frequency range as indicated in the rightmost plot.

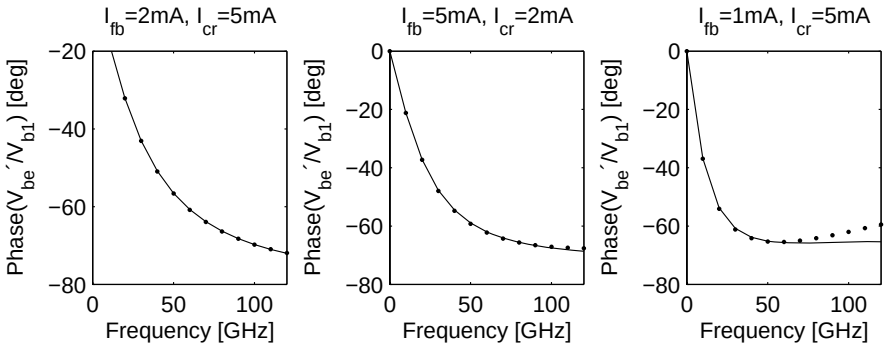

Figure C.2: Exact phase (-) and phase approximated by eq.(C.15) (··) at three different combinations of the bias currents.

Bibliography

[1] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. DenBaars, J. Speck, and U. Mishra, "High-power algan/gan hemts for ka-band applications," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 781–783.

[2] J. Das, J. Derluyn, A. Lorenz, H. Oprins, D. Xiao, W. De Raedt, K. Cheng, M. Leys, S. Degroote, M. Germain, and G. Borghs, "Gan technology on high-resistivity si-substrates for high-power-amplifiers," *ESA, Microwave Technology and Techniques Workshop*, 2008.

[3] L. Shen, T. Palacios, C. Poblenz, A. Corrion, A. Chakraborty, N. Fichtenbaum, S. Keller, S. Denbaars, J. Speck, and U. Mishra, "Unpassivated high power deeply recessed gan hemts with fluorine-plasma surface treatment," *IEEE Electron Device Letters*, vol. 27, no. 4, pp. 214–216, 2006.

[4] R. Lossy, N. Chaturvedi, P. Heymann, K. Köhler, S. Müller, and J. Würfl, "Algan/gan hemts on silicon carbide substrates for microwave power operation," *GaAs ManTech*, 2003.

[5] V. Krozer. Private communication, 2008.

[6] J. Wiltse, "Corrections to published curves for atmospheric attenuation in the 10 to 1000 ghz region," *IEEE Antennas and Propagation Society International Symposium 1997. Digest*, vol. 4, pp. 2580–2583 vol.4, 1997.

[7] G. Weibel and H. Dressel, "Propagation studies in millimeter-wave link systems," *Proceedings of the IEEE*, vol. 55, no. 4, pp. 497–513, 1967.

[8] C. Karnfelt, P. Hallbjorner, H. Zirath, and A. Alping, "High gain active microstrip antenna for 60-ghz wlan/wpan applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2593–2603, 2006.

[9] G. Boeck, V. Subramanian, W. Keusgen, and V. H. Do, "60 ghz sige hbt chip set for high speed wireless communication systems," *EuMC/EuMIC Workshop WTH-11: Modelling, Circuit Design and Measurement Techniques for Millimeter Wave Systems*, 2006.

[10] V. Dyadyuk, O. Sevimli, J. Bunton, J. Pathikulangara, and L. Stokes, "A 6 gbps millimetre wave wireless link with 2.4 bit/hz spectral efficiency," *2007 IEEE/MTT-S IMS*, pp. 471–474, 2007.

[11] T. K. Johansen. Private communication, 2006.

[12] K. Lee, J. Edie, R. Krueger, J. Weber, T. Brott, and W. Craig, "A low profile x-band active phased array for submarine satellite communications," *Proceedings 2000 IEEE International Conference on Phased Array Systems and Technology*, pp. 231–234, 2000.

[13] Y.-B. Jung, S.-Y. Eom, S.-I. Jeon, C.-J. Kim, and S.-O. Park, "T/rx channel design of x-band shipboard apaa system for mobile communications via satellite," *European Microwave Conference, 2003*, pp. 527–530, 2003.

[14] R. Tahim, J. Foshee, and K. Chang, "Multi-band phased array antennas for air-platforms," *IEEE Antennas and Propagation Society, AP-S International Symposium (Digest)*, vol. 4, pp. 204–207, 2002.

[15] J. C. Chen, L. Cooper, D. Taggart, N. S. Wagner, R. Kumar, T. Nguyen, J. Yoh, G. Leon, and G. W. Goo, "Performance of mpsk and 16qam in the satellite communication environment," *IEEE Aerospace Conference Proceedings*, vol. 2, pp. 1383–1390, 2004.

[16] A. Ghorbani and M. Sheikhan, "The effect of solid state power amplifiers (sspas) nonlinearities on mpsk and m-qam signal transmission," *Sixth International Conference on Digital Processing of Signals in Communications*, pp. 193–197, 1991.

[17] H. Takasu, F. Sadaki, M. Kawano, and S. Kamihashi, "Ka-band low loss and high power handling gaas pin diode mmic phase shifter for reflected-type phased array systems," *1999 IEEE MTT-S IMS Digest*, vol. 2, pp. 467–470 vol.2, 1999.

[18] International Manufacturing Services, *Application notes: Thick Film Two Way Wilkinson Power Divider - (www.ims-resistors.com)*.

[19] S. Piotrowicz, E. Chartier, J. Jacquet, D. Floriot, J. Obregon, P. Dueme, J. Delaire, and Y. Mancuso, "Ultra compact x-band gainp/gaas hbt mmic amplifiers : 11w, 42% of pae on 13mm and 8.7w, 38% of pae on 9mm," *IEEE MTT-S IMS Digest*, pp. 1867–1870, 2006.

[20] Z. Ouarch, "X-band gainp hbt 10 w high power amplifier including on-chip bias control circuit," *IEEE MTT-S IMS Digest*, vol. 2, pp. 855–858, 2003.

[21] F. Lenk, H. Klockenhoff, P. Kurpas, A. Maabdorf, H. Wurfl, and W. Heinrich, "A 3.2 w coplanar single-device x-band amplifier with gaas hbt," *2005 13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, pp. 49–52, 2006.

[22] K. Riepe, H. Leier, U. Seiler, A. Marten, and H. Sledzik, "High-efficiency gainp/gaas hbt mmic power amplifier with up to 9 w output power at 10 ghz," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 1, pp. 22–24, 1996.

[23] M. Khatibzadeh, B. Bayraktaroglu, and T. Kim, "12 w monolithic x-band hbt power amplifier," *IEEE, Microwave and Millimeter-Wave Monolithic Circuits Symposium, Digest of Papers*, pp. 47–50, 1992.

[24] J. Komiak and L. Yang, "5 watt high efficiency wideband 7 to 11 ghz hbt mmic power amplifier," *IEEE, Microwave and Millimeter-Wave Monolithic Circuits Symposium, Digest of Papers*, pp. 17–20, 1995.

[25] C.-K. Chu, H.-K. Huang, H.-Z. Liu, C.-H. Lin, C.-H. Chang, C.-L. Wu, C.-S. Chang, and Y.-H. Wang, "A 9.1-10.7 ghz 10 w, 40 db gain four-stage phemt mmic power amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 2, p. 151, 2007.

[26] A. Bessemoulin, M. Quay, S. Ramberger, and M. Schlechtweg, "A 4-watt x-band compact coplanar high power amplifier mmic with 18-db gain and 25-% pae," *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2002. 24th Annual Technical Digest*, pp. 189–192, 2002.

[27] C. Chu, H. Huang, H. Liu, R. Chiu, C. Lin, C. Wang, Y. Wang, C. Hsu, W. Wu, C. Wu, and C. Chang, "A fully matched 8w x-band phemt mmic high power amplifier," *IEEE, CSIC, Technical Digest*, pp. 137–140, 2004.

[28] P. Colantonio, F. Giannini, R. Giofre, E. Limiti, C. Lanzieri, and S. Lavanga, "A two stage high frequency class f power amplifier," *INMMIC 2007 - Proceedings*, pp. 187–190 and 4062294, 2007.

[29] M. Van Heijningen, A. De Boer, J. Hoogland, M. Van Wanum, A. De Hek, F. Van Vliet, and H. Brouzes, "Multi function and high power amplifier chipset for x-band phased array frontends," *EuMIC 2006 - Proceedings*, pp. 237–240, 2007.

[30] S. Chu, A. Platzker, M. Borkowski, R. Mallavarpu, M. Snow, A. Bowlby, D. Teeter, T. Kazior, and K. Alavi, "A 7.4 to 8.4 ghz high efficiency phemt three-stage power amplifier," *IEEE 2000 MTT-S IMS Digest*, vol. 2, pp. 947–950, 2000.

[31] H. Klockenhoff, R. Behtash, J. Wurfl, W. Heinrich, and G. Trankle, "A compact 16 watt x-band gan-mmic power amplifier," *IEEE MTT-S IMS Digest*, pp. 1846–1849, 2006.

[32] F. van Raay, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, R. Quay, R. Kiefer, F. Benkhelifa, B. Raynor, W. Pletschen, M. Kuri, H. Massler, and S. Muller, "A coplanar x-band algan/gan power amplifier mmic on s.i. sic substrate," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 7, pp. 460–462, 2005.

[33] P. Schuh, R. Kiefer, R. Leberer, H. Sledzik, M. Oppermann, B. Adelseck, H. Brugger, R. Behtash, H. Leier, and R. Quay, "20w gan hpas for next generation x-band t/r-modules," *IEEE MTT-S IMS Digest*, pp. 726–729, 2006.

[34] S. Sheppard, R. Smith, W. Pribble, Z. Ring, T. Smith, S. Allen, J. Milligan, and J. Palmour, "High power hybrid and mmic amplifiers using wide-bandgap semiconductor devices on semi-insulating sic substrates," *60th DRC. Conference Digest*, pp. 175–178, 2002.

[35] F. van Raay, R. Quay, R. Kiefer, W. Bronner, M. Seelmann-Eggebert, M. Schlechtweg, M. Mikulla, and G. Weimann, "X-band high-power microstrip algan/gan hemt amplifier mmics," *IEEE MTT-S IMS Digest*, pp. 1368–1371, 2006.

[36] D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, and J. J.W., "25 w x-band gan on si mmic," *GaAs Man.Tech. Digest*, 2005.

[37] D. Johnson and S. Raman, "A packaged sige x2 sub-harmonic mixer for u-nii band applications," *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 159–162, 2001.

[38] R. Kodkani and L. Larson, "An integrated 50-ghz sige sub-harmonic mixer/downconverter with a quadrature ring vco," *2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, p. 4 pp., 2006.

[39] K. Nimmagadda and G. Rebeiz, "A 1.9 ghz double-balanced subharmonic mixer for direct conversion receivers," *2001 IEEE RFIC Symposium*, pp. 253–256, 2001.

[40] Hittite Microwave Corporation, *Application notes: SUBHARMONIC vs. FUNDAMENTAL MIXERS FOR HIGH CAPACITY MILLIMETERWAVE RADIOS - (www.hittite.com)*.

[41] B. Razavi, *RF Microelectronics*. Prentice Hall PTR, 1998.

[42] J. Craninckx, V. Gravot, and S. Donnay, "A harmonic quadrature lo generator using a 90^o delay-locked loop," *ESSCIRC 2004 - Proceedings*, pp. 127–130, 2004.

[43] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-K. Yu, "Subharmonically pumped cmos frequency conversion (up and down) circuits for 2-ghz wcdma direct-conversion transceiver," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, 2004.

[44] D. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[45] F. Ellinger and H. Jackel, "38-43 ghz quadrature vco on 90 nm vlsi cmos with feedback frequency tuning," *IEEE MTT-S IMS Digest*, vol. 2005, pp. 1701–1703 and 1517042, 2005.

[46] M. Usama and T. A. Kwasniewski, "A 40 ghz quadrature lc vco and frequency divider in 90-nm cmos technology," *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 3047–3050 and 4253321, 2007.

[47] M. Sanduleanu and E. Stikvoort, "Highly linear, varactor-less, 24ghz iq oscillator," *RFIC) Symposium, Digest of Papers*, pp. 577–580, 2005.

[48] W. Chan, H. Veenstra, and J. Long, "A 32ghz quadrature lc-vco in 0.25ţm sige bicmos technology," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 48, pp. 448–449 and 29.5, 2005.

[49] S. Hackl, J. Bock, G. Ritzberger, M. Wurzer, and A. L. Scholtz, "A 28-ghz monolithic integrated quadrature oscillator in sige bipolar technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 135–137, 2003.

[50] E. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Review*, vol. 26, no. 2, pp. 163–177, 1965.

[51] M. Micovic, A. Kurdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. Willadsen, W. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel, and D. Chow, "Gan hfet for w-band power applications," *International Electron Devices Meeting*, pp. 1–3, 2006.

[52] A. Komijani and A. Hajimiri, "A wideband 77ghz, 17.5dbm power amplifier in silicon," *IEEE Proceedings, Custom Integrated Circuits Conference*, pp. 571–574, 2005.

[53] T. Ishibashi, "Nonequilibrium electron transport in hbts," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, p. 2595, 2001.

[54] H. Wang, R. Lai, M. Biedenbender, G. Dow, and B. Allen, "Novel w-band monolithic push-pull power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 10, pp. 1055–1061, 1995.

[55] R. Lai, R. Grundbacher, M. Barsky, A. Oki, M. Siddiqui, B. Pitman, R. Katz, P. Tran, L. Callejo, and D. Streit, "Extremely high p1db mmic amplifiers for ka-band applications," *2001 IEEE GaAs IC Symposium - Technical Digest*, pp. 115–17, 2001.

[56] J. Komiak, W. Kong, and K. Nichols, "High efficiency wideband 6 to 18 ghz phemt power amplifier mmic," *2002 IEEE MTT-S International Microwave Symposium Digest (Cat. No.02CH37278)*, pp. 905–7 vol.2, 2002.

[57] S.-W. Chen, P. Smith, S.-M. Liu, W. Kopp, and T. Rogers, "A 60-ghz high efficiency monolithic power amplifier using 0.1-μm phemt's," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 6, pp. 201–203, 1995.

[58] F. Y. Colomb and A. Platzker, "A 3-watt q-band gaas phemt power amplifier mmic for high temperature operation," *IEEE MTT-S IMS Digest*, pp. 897–900, 2006.

[59] P. M. Smith, S.-M. J. Liu, M.-Y. Kao, P. Ho, S. C. Wang, K. H. G. Duh, S. T. Fu, and P. C. Chao, "W-band high efficiency inp-based power hemt with 600 ghz f_{max}," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 7, pp. 230–232, 1995.

[60] L. Samoska, A. Peralta, M. Hu, M. Micovic, and A. Schmitz, "A 20 mw, 150 ghz inp hemt mmic power amplifier module," *Microwave and Wireless Components Letters, IEEE*, vol. 14, no. 2, pp. 56–58, 2004.

[61] S. Liu, O. Tang, W. Kong, K. Nichols, J. Heaton, and P. Chao, "High efficiency monolithic inp hemt v-band power amplifier," *GaAs IC Symposium, 1999*, pp. 145–147, 1999.

[62] P. Huang, R. Lai, R. Grundbacher, and B. Gorospe, "A 20-mw g-band monolithic driver amplifier using 0.07-μm inp hemt," *IEEE 2006 MTT-S IMS Digest*, pp. 806–809, 2006.

[63] W. Deal, X. Mei, V. Radisic, M. Lange, W. Yoshida, L. Po-hsin, J. Uyeda, M. Barsky, A. Fung, T. Gaier, and R. Lai, "Development of sub-millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 122, pp. 2719–2726.

[64] K. Herrick, S. Lardizabal, P. Marsh, and C. Whelan, "95 ghz metamorphic hemt power amplifiers on gaas," *2003 IEEE MTT-S IMS Digest*, vol. 1, pp. 137–140 vol.1, 2003.

[65] P. Smith, D. Dugas, K. Chu, K. Nichols, K. Duh, J. Fisher, L. Mt Pleasant, D. Xu, L. Gunter, A. Vera, R. Lender, and D. Meharry, "Progress in gaas metamorphic hemt technology for microwave applications," *ESSDERC 2003 - Proceedings*, pp. 21–24, 2003.

[66] D. M. Kang, J. Y. Hong, J. Y. Shim, J.-H. Lee, H.-S. Yoon, and K. H. Lee, "A 77 ghz mhemt mmic chip set for automotive radar systems," *ETRI Journal*, vol. 27, no. 2, pp. 133–139, 2005.

[67] M. Salib, A. Gupta, F. Ali, and D. Dawson, "1.8-W, 6-18-GHz HBT MMIC power amplifier with 10-dB gain and 37% peak power-added efficiency," *IEEE Microwave and Guided Wave Letters*, vol. 3, no. 9, pp. 325–326, 1993.

[68] S. Tanaka, S. Yamanouchi, Y. Amamiya, T. Niwa, K. Hosoya, H. Shimawaki, and K. Honjo, "A ka-band hbt mmic power amplifier," *2000 IEEE MTT-S IMS Digest*, pp. 553–6 vol.1, 2000.

[69] K. Kobayashi, A. Oki, L.-W. Yang, A. Gutierrez-Aitken, P. Chin, D. Sawdai, W. Okamura, J. Lester, E. Kaneshiro, P. Grossman, K. Sato, T. Block, H. Yen, and D. Streit, "A 0.5 watt-40% pae inp double heterojunction bipolar transistor k-band mmic power amplifier," *International Conference on Indium Phosphide and Related Materials - Proceedings*, pp. 250–253, 2000.

[70] V. Paidi, Z. Griffith, Y. Wei, M. Dahlstrom, M. Urteaga, N. Parthasarathy, M. Seo, L. Samoska, A. Fung, and M. Rodwell, "G-band (140-220 ghz) and w-band (75-110 ghz) inp dhbt medium power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 598–605, 2005.

[71] G. Ellis, A. Kurdoghlian, R. Bowen, M. Wetzel, and M. Delaney, "W-band inp dhbt mmic power amplifiers," *2004 IEEE MTT-S IMS Digest*, vol. 1, pp. 231–234, 2004.

[72] T. Quach, W. Okamura, A. Gutierrez-Aitken, T. Jenkins, E. Kaneshiro, L. Kehias, A. Oki, D. Sawdai, P. Watson, R. Welch, R. Worley, and H. Yen, "Ultra-efficient x-band and linear-efficient ka-band power amplifiers using indium phosphide double heterojunction bipolar transistors," *Conference Proceedings - International Conference on Indium Phosphide and Related Materials*, pp. 501–504, 2001.

[73] V. Paidi, Z. Griffith, Y. Wei, M. Dahlstrom, N. Parthasarathy, M. Urteaga, M. Rodwell, A. Fung, and L. Samoska, "Common base amplifier with 7-db gain at 176 ghz in inp mesa dhbt technology," *2004 IEEE RFIC Symposium - Digest of Papers*, pp. 189–192, 2004.

[74] L. Yang, K. Kobayashi, D. Steit, A. Oki, H. Yen, P. Grossman, T. Block, L. Tran, A. Gutierrez-Aitken, L. Callejo, J. Macek, and S. Maas, "High linearity k-band inp hbt power amplifier mmic with 62.8% pae at 21 ghz," *IEEE 1999 GaAs IC Symposium - Technical Digest*, pp. 73–76, 1999.

[75] J. Hacker, W. Ha, C. Hillman, M. Urteaga, R. Pierson, and B. Brar, "Compact inp hbt power amplifiers using integrated thick bcb dielectrics," *2007 IEEE MTT-S IMS*, pp. 805–808, 2007.

[76] P. Huang, E. Lin, R. Lai, M. Biedenbender, T. Huang, H. Wang, C. Geiger, T. Block, and P. Liu, "A 94 ghz monolithic high output power amplifier," *1997 IEEE MTT-S IMS Digest*, no. vol.3, pp. 1175–8, 1997.

[77] O. Tang, K. Duh, S. Liu, P. Smith, W. Kopp, T. Rogers, and D. Pritchard, "Design of high-power, high-efficiency 60-ghz mmics using an improved nonlinear phemt model," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1326–1333, 1997.

[78] D. Ingram, Y. Chen, J. Kraus, B. Brunner, B. Allen, H. Yen, and K. Lau, "A 427 mw, 20% compact w-band inp hemt mmic power amplifier," *1999 IEEE RFIC Symposium*, pp. 95–98, 1999.

[79] M. Yu, M. Matloubian, P. Petre, L. Hamilton, R. Bowen, M. Lui, H. Sun, C. Ngo, P. Janke, D. Baker, and R. Robertson, "W-band inp-based hemt mmic power amplifiers using finite-ground cpw design," *Technical Digest - GaAs IC Symposium*, pp. 37–40, 1998.

[80] Y. C. C. et al., "A single chip 1-w inp hemt v-band module," *GaAs IC Symposium, 1999. 21st Annual*, pp. 149–152, 1999.

[81] A. Tessmann, A. Leuther, C. Schwoerer, and H. Massler, "Metamorphic 94 ghz power amplifier mmics," *2005 IEEE MTT-S IMS Digest*, p. 4 pp., 2005.

[82] Y. Wei, M. Urteaga, Z. Griffith, D. Scott, S. Xie, V. Paidi, N. Parthasarathy, and M. Rodwell, "75 ghz 80 mw inp dhbt power amplifier," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 919–921, 2003.

[83] T. O'Sullivan, M. Le, P. Partyka, R. Milano, and P. Asbeck, "Design of a 70 ghz power amplifier using a digital inp hbt process," *2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 214–217, 2007.

[84] U. R. Pfeiffer, S. K. Reynolds, and B. A. Floyd, "A 77 ghz sige power amplifier for potential applications in automotive radar systems," *Digest of Papers - 2004 IEEE RFIC Symposium*, pp. 91–94, 2004.

[85] U. Pfeiffer, "A 20dbm fully-integrated 60ghz sige power amplifier with automatic level control," *Proceedings - ESSCIRC (IEEE Cat. No. 06EX1347)*, pp. 356–9, 2006.

[86] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, "An electrical funnel: a broadband signal combining method," *Solid-State Circuits, IEEE International Conference Digest of Technical Papers*, p. 10 pp., 2006.

[87] V.-H. Do, V. Subramanian, W. Keusgen, and G. Boeck, "A 60 ghz sige-hbt power amplifier with 20% pae at 15 dbm output power," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 3, pp. 209–211, 2008.

[88] U. R. Pfeiffer and D. Goren, "A 23-dbm 60-ghz distributed active transformer in a silicon process technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 857–865, 2007.

[89] M. Rodwell, M. Urteaga, Y. Betser, T. Mathew, P. Krishnan, D. Scott, S. Jaganathan, D. Mensa, J. Guthrie, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, and S. Long, "Scaling of ingaas/inalas hbts for high speed mixed-signal and mm-wave ics," *International Journal of High Speed Electronics and Systems*, vol. 11, no. 1, pp. 159–215, 2001.

[90] F. Colomb and A. Platzker, "2 and 4 watt ka-band gaas phemt power amplifier mmics," *2003 IEEE MTT-S IMS Digest*, pp. 843–846 vol.2, 2003.

[91] R. Kasody, G. Dow, A. Sharma, M. Aust, D. Yamauchi, R. Lai, M. Biedenbender, K. Tan, and B. Allen, "A high efficiency v-band monolithic hemt power amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 4, no. 9, pp. 303–304, 1994.

[92] C. Lin, H. Liu, C. Chu, H. Huang, Y. Wang, C. Liu, C. Chang, C. Wu, and C. Chang, "A fully matched ku-band 9w phemt mmic high power amplifier," *Compound Semiconductor Integrated Circuit Symposium, 2006 IEEE*, pp. 165–168, 2006.

[93] L. Samoska and Y. C. Leong, "65-145 ghz inp mmic hemt medium power amplifiers," *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, pp. 1805–1808 vol.3, 2001.

[94] F. Lam, M. Matloubian, A. Igawa, C. Chou, A. Kurdoghlian, C. Ngo, L. Jelloian, A. Brown, M. Thompson, and L. Larson, "44-ghz high-efficiency inp-hemt mmic power amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 4, no. 8, pp. 277–278, 1994.

[95] P. J. Bartusiak, T. Henderson, T. Kim, and B. Bayraktaroglu, "High-efficiency ku-band hbt mmic power amplifier," *IEEE Electron Device Letters*, vol. 13, no. 11, pp. 584–586, 1992.

[96] Y. Wei, K. Sundararajan, M. Urteaga, Z. Griffith, D. Scott, V. Paidi, N. Parthasarathy, and M. Rodwell, "40 ghz mmic power amplifier in inp dhbt technology," *Proceedings IEEE Lester Eastman Conference on High Performance Devices*, pp. 352–357, 2002.

[97] A. Schott, H. Kuhnert, F. Lenk, J. Hilsenbeck, J. Wurfl, and W. Heinrich, "38 ghz push-push gaas-hbt mmic oscillator," *2002 IEEE MTT-S IMS Digest*, no. vol.2, pp. 839–42 vol.2, 2002.

[98] F. Lenk, M. Schott, J. Hilsenbeck, and W. Heinrich, "Low phase-noise gaas-hbt monolithic w-band oscillator," *2004 EuMC*, vol. 2, pp. 897–900.

[99] M. Bao, Y. Li, and H. Jacobsson, "A 25-ghz ultra-low phase noise ingap/gaas hbt vco," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 11, pp. 751–753, 2005.

[100] A. Inoue, H. Amasuga, S. Watanabe, S. Goto, and T. Oku, "Mmic technologies for mw and mmw applications," *2007 IEEE International Workshop on Radio-Frequency Integration Technology*, pp. 232–235, 2007.

[101] K. Uchida, I. Aoki, H. Matsuura, T. Yakihara, S. Kobayashi, S. Oka, T. Fujita, and A. Miura, "104 and 134 ghz ingap/ingaas hbt oscillators," *IEEE GaAs IC Symposium - Technical Digest*, pp. 237–240, 1999.

[102] T. Kashiwa, T. Ishida, T. Katoh, H. Kurusu, H. Hoshi, and Y. Mitsui, "V-band high-power low phase-noise monolithic oscillators and investigation of low phase-noise performance high drain bias," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 102, pp. 1559–1565, 1998.

[103] S. Kudszus, T. Berceli, A. Tessmann, M. Neumann, and W. Haydl, "W-band hemt-oscillator mmics using subharmonic injection locking," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2526–2532, 2000.

[104] J. Lin, Y. Chen, D. Humphrey, R. Hamm, R. Malik, A. Tate, R. Kopf, and R. Ryan, "Ka-band monolithic ingaas/inp hbt vco's in cpw structure," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 11, pp. 379–381, 1995.

[105] Z. Lao, J. Jensen, K. Guinn, and M. Sokolich, "80-ghz differential vco in inp shbts," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 9, pp. 407–409, 2004.

[106] H. Wang, K. W. Chang, L. T. Tran, J. C. Cowles, T. R. Block, E. W. Lin, G. S. Dow, A. K. Oki, D. C. Streit, and B. R. Allen, "Low phase noise millimeter-wave frequency sources using inp-based hbt mmic technology," *IEEE Journal of Solid State Circuits - Institute of Elect and Electr Engineers*, vol. 31, no. 10, p. 1419, 1996.

[107] K. Kobayashi, A. Oki, L. Tran, J. Cowles, A. Gutierrez-Aitken, F. Yamada, T. Block, and D. Streit, "A 108-ghz inp-hbt monolithic push-push vco with low phase noise and wide tuning bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 9, pp. 1225–1232, 1999.

[108] Y. Baeyens, C. Dorschky, N. Weimann, Q. Lee, R. Kopf, G. Georgiou, J.-P. Mattia, R. Hamm, and Y.-K. Chen, "Compact inp-based hbt vcos with a wide tuning range at w- and d-band," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2403–2408, 2000.

[109] R. Wanner, R. Lachner, and G. Olbrich, "Sige integrated mm-wave push-push vcos with reduced power consumption," *IEEE RFIC Symposium, 2006*, p. 4 pp., 2006.

[110] S. Trotta, H. Knapp, K. Aufinger, T. Meister, J. Bock, W. Simburger, and A. Scholtz, "A fundamental vco with integrated output buffer beyond 120 ghz in sige bipolar technology," *2007 IEEE/MTT-S IMS*, pp. 645–648, 2007.

[111] H. Li and H.-M. Rein, "Millimeter-wave vcos with wide tuning range and low phase noise, fully integrated in a sige bipolar production technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 184–191, 2003.

[112] Y. Wachi, T. Nagasaku, and H. Kondoh, "A 28ghz low-phase-noise cmos vco using an amplitude-redistribution technique," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pp. 482–630, 2008.

[113] G. Le Grand de Mercey, "A 18ghz rotary traveling wave vco in cmos with i/q outputs," *ESSCIRC 2004*, pp. 489–492, 2003.

[114] J.-C. Chien and L.-H. Lu, "40ghz wide-locking-range regenerative frequency divider and low-phase-noise balanced vco in 0.18ţm cmos," *2007 IEEE International Solid-State Circuits Conference*, pp. 544–621, 2007.

[115] D. Huang, W. Hant, N.-Y. Wang, T. Ku, Q. Gu, R. Wong, and M.-C. Chang, "A 60ghz cmos vco using on-chip resonator with embedded artificial dielectric for size, loss and noise reduction," *2006 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, p. 10 pp., 2006.

[116] C. Cao, E. Seok, and K. K. O, "Millimeter-wave cmos voltage-controlled oscillators," *2007 IEEE Radio and Wireless Symposium*, pp. 185–188, 2007.

[117] M. Yu, R. J. Ward, R. A. Newgard, and M. Urteaga, "A compact 43-ghz monolithic differential vco in 0.5-ţm inp dhbt technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 281–283, 2006.

[118] D. Hadziabdic, "Low voltage, low noise l-band vco design," Master's thesis, Technical University of Denmark, DK-2800 Kgs. Lyngby, 2005.

[119] F.-H. Huang, C.-K. Lin, and Y.-J. Chan, "V-band gaas phemt cross-coupled sub-harmonic oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 8, pp. 473–475, 2006.

[120] D. M. Pozar, *Microwave Engineering*. John Wiley & Sons, 2 ed., 1998.

[121] V. Radisic, X. B. Mei, W. R. Deal, W. Yoshida, P. H. Liu, J. Uyeda, M. Barsky, L. Samoska, A. Fung, T. Gaier, and R. Lai, "Demonstration of sub-millimeter wave fundamental oscillators using 35-nm inp hemt technology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 223–225, 2007.

[122] V. Radisic, D. Sawdai, D. Scott, W. Deal, L. Dang, D. Li, J. Chen, A. Fung, L. Samoska, T. Gaier, and R. Lai, "Demonstration of a 311-ghz fundamental oscillator using inp hbt technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 11, pp. 2329–2335, 2007.

[123] M. Kraemer, *Gallium nitride-based microwave high-power heterostructure field-effect transistors : design, technology, and characterization*. PhD thesis, Technische Universiteit Eindhoven, 2006.

[124] A. Bessemoulin, W. Marsetz, Y. Baeyens, R. Osorio, H. Massler, A. Hulsmann, and M. Schlechtweg, "Design of coplanar power amplifiers for mm-wave system applications including thermal aspects," *GAAS 2000. Conference Proceedings*, p. 4 pp., 2000.

[125] N. Chaturvedi. Private communication, 2008.

[126] F. Giannini, G. Leuzzi, E. Limiti, and L. Scucchia, "Design-oriented non-linear analysis of class-ab power amplifiers," *IEEE MTT-S IMS Digest*, pp. 297–300 vol.1, 1993.

[127] H. C. Casey, *Device for Integrated Circuits: Silicon and III-V Compound Semiconductors*. John Wiley & Sons, 1999.

[128] P. Houston, "High-frequency heterojunction bipolar transistor device design and technology," *Electronics and Communication Engineering Journal*, vol. 12, no. 5, pp. 220–228, 2000.

[129] H. Kroemer, "Heterostructure bipolar transistors: what should we build?," *Journal of Vacuum Science and Technology B (Microelectronics Processing and Phenomena)*, vol. 1, no. 2, pp. 126–30, 1983.

[130] D. Harame, J. Comfort, J. Cressler, E. Crabbe, J.-C. Sun, B. Meyerson, and T. Tice, "Si/sige epitaxial-base transistors. i. materials, physics, and circuits," *IEEE Transactions on Electron Devices*, vol. 42, no. 3, pp. 455–468, 1995.

[131] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Artech House, 2003.

[132] J. Kirk, C.T., "A theory of transistor cutoff frequency (ft) falloff at high current densities," *IEEE Transactions on Electron Devices*, vol. 9, no. 2, pp. 164–174, 1962.

[133] S. Blayac, M. Riet, J. Benchimol, P. Berdaguer, N. Kauffman, J. Godin, and A. Scavennec, "Lateral design of inp/ingaas dhbts for 40 gbit/s ics," *Conference Proceedings. International Conference on Indium Phosphide and Related Materials (Cat. No.00CH37107)*, pp. 481–484, 2000.

[134] S. Blayac, M. Riet, J. Benchimol, F. Alexandre, P. Berdaguer, M. Kahn, A. Pinquier, E. Dutisseuil, J. Moulu, A. Kasbari, A. Konczykowska, and J. Godin, "Msi inp/ingaas dhbt technology: beyond 40 gbit/s circuits," *Conference Proceedings. 14th Indium Phosphide and Related Materials Conference (Cat. No.02CH37307)*, pp. 51–54, 2002.

[135] J. Godin, M. Riet, P. Berdaguer, V. Nodjiadjim, A. Konczykowska, and A. Scavennec, "Inp dhbt technology development for high bitrate mixed-signal ic fabrication," *International Conference on Indium Phosphide and Related Materials Conference Proceedings (IEEE Cat. No.06CH37737C)*, pp. 258–61, 2006.

[136] J. Godin, P. Andre, J. Benchimol, P. Berdaguer, S. Blayac, J. Burie, P. Desrousseaux, A. Duchenois, N. Kauffmann, A. Konczykowska, and M. Riet, "40 gbit/s optical communications: Inp dhbt technology, circuits and system experiments," *Technical Digest - GaAs IC Symposium (Gallium Arsenide Integrated Circuit)*, pp. 185–188, 1999.

[137] A. Konczykowska, F. Jorge, M. Riet, J. Moulu, and J. Godin, "50 gb/s dff and decision circuits in inp dhbt technology for etdm systems," *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, pp. 605–7, 2006.

[138] J. Godin, V. Nodjiadjim, M. Riet, P. Berdaguer, O. Drisse, E. Derouin, A. Konczykowska, J. Moulu, J.-Y. Dupuy, F. Jorge, J.-L. Gentner, A. Scavennec, T. Johansen, and V. Krozer, "Submicron inp dhbt technology for high-speed high-swing mixed-signal ics," *2008 IEEE Compound Semiconductor Integrated Circuits Symposium*, pp. 1–4, 2008.

[139] T. Johansen, V. Krozer, A. Konczykowska, M. Riet, and J. Vidkjaer, "Large-signal modeling of high-speed inp dhbts using electromagnetic simulation based de-embedding," *IEEE MTT-S IMS Digest*, pp. 655–658, 2006.

[140] B. Heinemann, R. Barth, D. Knoll, H. Rücker, B. Tillack, and W. Winkler, "High-performance bicmos technologies without epitaxially-buried subcollectors and deep trenches," *Semiconductor Science and Technology*, vol. 22, no. 1, pp. S153–S157, 2007.

[141] G. G. Fischer. Private communication, 2006.

[142] V. Parthasarathy, R. Zhu, V. Khemka, T. Roggenbauer, A. Bose, P. Hui, P. Rodriquez, J. Nivison, D. Collins, Z. Wu, I. Puchades, and M. Butner, "A 0.25 μm cmos based 70v smart power technology with deep trench for high-voltage isolation," *Digest. International Electron Devices Meeting,*, pp. 459–462.

[143] M. Khater, J.-S. Rieh, T. Adam, A. Chinthakindi, J. Johnson, R. Krishnasamy, M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K. Schonenberg, P. Smith, K. Stein, A. Stricker, S.-J. Jeng, and et al., "Sige hbt technology with fmax/ft = 350/300 ghz and gate delay below 3.3 ps," *Technical Digest - IEDM*, pp. 247–250, 2004.

[144] B. Barbalat, T. Schwartzmann, P. Chevalier, T. Jagueneau, B. Vandelle, L. Rubaldo, F. Saguin, N. Zerounian, F. Aniel, and A. Chantre, "Deep trench isolation effect on self-heating and rf performances of sigec hbts," *Proceedings of 35th European Solid-State Device Research Conference, 2005. ESSDERC 2005.*, pp. 129–132.

[145] F. Raab, "Maximum efficiency and output of class-f power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1162–1166, 2001.

[146] I. Bahl, E. Griffin, A. Geissberger, C. Andricos, and T. Brukiewa, "Class-b power mmic amplifiers with 70 percent power-added efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1315–1320, 1989.

[147] J. Wurfl, R. Behtash, R. Lossy, A. Liero, W. Heinrich, G. Trankle, K. Hirche, and G. Fischer, "Advances in gan-based discrete power devices for l- and x-band applications," *1st European Microwave Integrated Circuits Conference*, p. 3 pp., 2006.

[148] J. Vidkjaer, *Class Notes, 31415 RF-Comm. Circ.*, ch. I, Modulation, Transmission, and Demodulation. DTU, 2004.

[149] J. Vidkjaer, *Class Notes, 31415 RF-Comm. Circ.*, ch. IV, Noise and Distortion. DTU, 2004.

[150] P. Banelli, G. Baruffa, and S. Cacopardi, "Effects of hpa non linearity on frequency multiplexed ofdm signals," *IEEE Transactions on Broadcasting*, vol. 47, no. 2, pp. 123–136, 2001.

[151] C. Seymour and A. Knight, "A performance comparison between state of the art gaas and gan power fets," *ESTEC, Proc of the Microwave Technology and Techniques Workshop: Enabling Future Space Systems*, 15-16 May 2006 (ESA SP-632).

[152] Y.-F. Wu, P. Chavarkar, M. Moore, P. Parikh, and U. Mishra, "Linearity and gain characteristics of algan/gan hemts," *Technical Digest - International Electron Devices Meeting*, pp. 697–699, 2002.

[153] N. De Carvalho and J. Pedro, "Large- and small-signal imd behavior of microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2364–2374, 1999.

[154] www.norsat.com, *GLOBETrekker X-Band.*

[155] www.xicomtech.com, *XTRS-200X-B1 X-Band Rack Mount SSPAs With Block Upconverter.*

[156] www.AdvantechAMT.com, *X-BAND HUB-MOUNT BLOCK-UP CONVERTER 80W TO 150W, SSPB-3000X series.*

[157] www.cpii.com/satcom, *CPI 2.25 and 2.50 kW SuperLinear TWT Amplifiers for Satellite Communications (TL22XI and TL25XI).*

[158] C. Moreno, M. Saura, D. Gómez, and R. Vilaseca, "A high efficiency 4w x-band phemt power hybrid for space application," *ESA, Microwave Technology and Techniques Workshop*, 6. May 2008.

[159] K. Iyomasa, K. Yamanaka, K. Mori, H. Noto, H. Ohtsuka, M. Nakayama, S. Yoneda, Y. Kamo, and Y. Isota, "Gan hemt 60w output power amplifier with over 50% efficiency at c-band 15% relative bandwidth using combined short and open circuited stubs," *IEEE MTT-S IMS Digest*, pp. 1255–1258, 2007.

[160] S. Xie, V. Paidi, R. Coffie, S. Keller, S. Heikman, B. Moran, A. Chini, S. DenBaars, U. Mishra, S. Long, and M. Rodwell, "High-linearity class b power amplifiers in gan hemt technology," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 7, pp. 284–6, 2003.

[161] J. Vidkjaer, *Class Notes, 31415 RF-Comm. Circ.*, ch. V, Power and Nonlinear RF-amplifiers. DTU, 2004.

[162] P. White, "Effect of input harmonic terminations on high efficiency class-b and class-f operation of phemt devices," *IEEE MTT-S IMS Digest (Cat. No.98CH36192)*, vol. 3, pp. 1611–1614 vol.3, 1998.

[163] P. M. White and T. M. O'Leary, "50% efficiency 8w c-band phemt power mmic amplifier," *Technical Digest - GaAs IC Symposium*, pp. 277–280, 1995.

[164] M. Maeda, H. Takehara, M. Nakamura, Y. Ota, and O. Ishikawa, "A high power and high efficiency amplifier with controlled second-harmonic source impedance," *IEEE MTT-S IMS Digest*, pp. 579–584, 1995.

[165] S. Watanabe, S. Takatuka, K. Takagi, H. Kuroda, and Y. Oda, "Simulation and experimental results of source harmonic tuning on linearity of power gaas fet under class ab operation," *IEEE MTT-S IMS Digest*, vol. 3, pp. 1771–1774, 1996.

[166] Y. Y. Woo, Y. Yang, I. Kim, and B. Kim, "Efficiency comparison between highly efficient class-f and inverse class-f power amplifiers," *IEEE Microwave Magazine*, vol. 8, no. 3, pp. 100–110, 2007.

[167] C. Roff, J. Benedikt, and P. J. Tasker, "Design approach for realization of very high efficiency power amplifiers," *IEEE MTT-S IMS Digest*, pp. 143–146, 2007.

[168] A. Grebennikov, "Circuit design technique for high efficiency class f amplifiers," *IEEE MTT-S IMS Digest (Cat. No.00CH37017)*, vol. 2, pp. 771–774 vol.2, 2000.

[169] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House, 1999.

[170] P. Schuh, R. Leberer, H. Sledzik, M. Oppermann, B. Adelseck, H. Brugger, R. Quay, M. Mikulla, and G. Weimann, "Advanced high power amplifier chain for x-band t/r-modules based on gan mmics," *The 1st European Microwave Integrated Circuits Conference*, pp. 241–244, 2006.

[171] F. van Raay, R. Quay, R. Kiefer, H. Walcher, O. Kappeler, M. Seelmann-Eggebert, S. Muller, M. Schlechtweg, and G. Weimann, "High power/high bandwidth gan mmics and hybrid amplifiers: design and characterization," *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, pp. 373–6, 2006.

[172] G. Gonzalez, *Micrwave transistor amplifiers, Analysis and design*. Prentice Hall, 2 ed., 1997.

[173] C. McAndrew, J. Seitchik, D. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. Roulston, M. Schroter, P. van Wijnen, and L. Wagner, "Vbic95, the vertical bipolar inter-company model," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1476–1483, 1996.

[174] T. K. Johansen, J. Vidkjaer, and V. Krozer, "Consistent large-signal modeling of sige hbt devices," in *Gallium Arsenide applications symposium*, 2004.

[175] A. Chakravorty, R. Scholz, D. Knoll, A. Fox, B. Senapati, and C. Maiti, "Implementation of a scalable vbic model for sige:c hbts," *Solid State Electronics*, vol. 50, no. 3, pp. 399–407, 2006.

[176] K. Lee, K. Choi, S.-H. Kook, D.-H. Cho, K.-W. Park, and B. Kim, "Direct parameter extraction of sige hbts for the vbic bipolar compact model," *IEEE Transactions on Electron Devices*, vol. 52, no. 3, pp. 375–384, 2005.

[177] H. Cho and D. Burk, "A three-step method for the de-embedding of high-frequency s-parameter measurements," *IEEE Transactions on Electron Devices*, vol. 38, no. 6, pp. 1371–1375, 1991.

[178] L. Tiemeijer and R. Havens, "A calibrated lumped-element de-embedding technique for on-wafer rf characterization of high-quality inductors and high-speed transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 822–829, 2003.

[179] T. Kolding, "A four-step method for de-embedding gigahertz on-wafer cmos measurements," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 734–740, 2000.

[180] T. K. Johansen, *Monolithic Microwave Integrated Circuits for Wideband SAR System*. PhD thesis, Technical University of Denmark, DK-2800 Kgs. Lyngby, 2003.

[181] T. Johansen, J. Vidkjaer, and V. Krozer, "Substrate effects in wideband sige hbt mixer circuits," *Gallium Arsenide applications symposium. GAAS 2003*, 2003.

[182] T. Johansen, V. Krozer, J. Vidkjaer, and T. Djurhuus, "Substrate effects in wideband sige hbt mixer circuits," *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, pp. 469–72, 2006.

[183] Y. Gobert, P. Tasker, and K. Bachem, "A physical, yet simple, small-signal equivalent circuit for the heterojunction bipolar transistor," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 1, pp. 149–153, 1997.

[184] C. A. King, J. L. Hoyt, and J. F. Gibbons, "Bandgap and transport properties of si1-xgex by analysis of nearly ideal si/si1-xgex/si heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2093–2104, 1989.

[185] G. Kull, L. Nagel, S.-W. Lee, P. Lloyd, E. Prendergast, and H. Dirks, "A unified circuit model for bipolar transistors including quasi-saturation effects," *IEEE Transactions on Electron Devices*, vol. 32, no. 6, pp. 1103–1113, 1985.

[186] C. Schippel, F. Schwierz, and J. Fu, "The influence of collector designs on fmax versus ft characteristics for different types of si-based rf bipolar transistors," *Semiconductor Science and Technology*, vol. 22, no. 1, pp. S76–S79, 2007.

[187] A. J. Joseph, J. D. Cressler, D. M. Richey, and G. Niu, "Optimization of sige hbt's for operation at high current densities," *IEEE Transactions on Electron Devices*, vol. 46, no. 7, pp. 1347–1354, 1999.

[188] "http://www.designers-guide.org/vbic/references.html."

[189] E. John, M. Das, L.-W. Yang, and S. Liu, "Extraction of high-frequency equivalent network parameters of hbt's by low-frequency extrapolation of microwave s-parameter data," *Proceedings. IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits (Cat. No.93CH3235-9)*, pp. 141–7, 1993.

[190] H. de Graaff, "State of the art in compact modelling with emphasis on bipolar rf circuit design," *27th European Solid-State Device Research Conference*, pp. 14–23.

[191] H. Li, H.-M. Rein, T. Suttorp, and J. Bock, "Fully integrated sige vcos with powerful output buffer for 77-ghz automotive radar systems and applications around 100 ghz," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1650–8, 2004.

[192] A. Konczykowska. Private communication, 2007.

[193] R. Arnold and D. Zoroglu, "A quantitative study of emitter ballasting," *International Electron Devices Meeting*, pp. 140–142, 1972.

[194] K. Mori, J. Nishihara, H. Utsumi, and M. Inoue, A. Miyazaki, "X-band 14w high efficiency internally-matched hfet," *IEEE MTT-S IMS Digest*, vol. 108, no. 1, pp. 59–62, 2008.

[195] J. Guthrie, M. Urteaga, D. Scott, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, Y. Betser, and M. Rodwell, "Hbt mmic 75 ghz and 78 ghz power amplifiers," *Conference Proceedings. International Conference on Indium Phosphide and Related Materials (Cat. No.00CH37107)*, pp. 246–9, 2000.

[196] A. Fung, L. Samoska, T. Gaier, V. Radisic, D. Sawdai, D. Scott, W. Deal, L. Dang, D. Li, A. Cavus, R. To, and R. Lai, "Demonstration of 184 and 255-ghz amplifiers using inp hbt technology," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 4, pp. 281–283, 2008.

[197] S. Tanaka, Y. Amamiya, S. Murakami, H. Shimawaki, N. Goto, Y. Takayama, and K. Honjo, "Design considerations for millimeter-wave power hbts based on gain performance analysis," *IEEE Transactions on Electron Devices*, vol. 45, no. 1, pp. 36–44.

[198] B. Bayraktaroglu and M. Salib, "Unconditionally thermally stable cascode gaas hbts for microwave applications," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 7, pp. 187–189.

[199] T. Morf, S. Hubscher, D. Huber, A. Huber, V. Schwarz, and H. Jackel, "98-ghz inp/ingaas hbt amplifier with 26-db gain," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 12, pp. 523–525, 1999.

[200] D. Walkey, D. Celo, T. Smy, and R. Surridge, "A thermal design methodology for multifinger bipolar transistor structures," *IEEE Transactions on Electron Devices*, vol. 49, no. 8, pp. 1375–1383, 2002.

[201] J. Li, P. Asbeck, T. Hussain, D. Hitko, C. Fields, and M. Sokolich, "Effects of device design on the thermal properties of hbts," *International Symposium on Compound Semiconductors: Post-Conference Proceedings (IEEE Cat. No.03TH8767)*, pp. 138–143, 2004.

[202] C. J. Reimer and T. Smy, "A simulation study of ic layout effects on thermal management of die attached gaas ics," *IEEE Transactions on Components and Packaging Technologies*, vol. 23, no. 2, p. 341, 2000.

[203] T. Becks and I. Wolff, "Full-wave analysis of various coplanar bends and t-junctions with respect to different types of air-bridges," *1993 IEEE MTT-S International Microwave Symposium Digest (Cat. No.93CH3277-1)*, pp. 697–700 vol.2, 1993.

[204] R. Kodkani and L. Larson, "A 25 ghz quadrature voltage controlled ring oscillator in 0.12ţm sige hbt," *2006 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (IEEE Cat. No.06EX1204)*, p. 4 pp., 2006.

[205] S.-H. Tarng and C. F. Jou, "A 10 ghz low power cmos quadrature voltage-controlled oscillator," *Proceedings, APMC*, vol. 2, p. 1606452, 2005.

[206] C. Cao and K. Kenneth, "Millimeter-wave voltage-controlled oscillators in 0.13-ţm cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304 and 1637594, 2006.

[207] D. Ghosh and R. Gharpurey, "A technique to extend tuning range of high frequency quadrature vco," *6th IEEE Dallas Circuits and Systems Workshop on System-on-Chip*, pp. 1–4, 2007.

[208] J. Kozikowski, "Analysis and design of emitter followers at high frequencies," *IEEE Transactions on Circuit Theory*, vol. CT-11, no. 1, pp. 129–136, 1964.

[209] L. Romano, S. Levantino, A. Bonfanti, C. Samori, and A. Lacaita, "Phase noise and accuracy in quadrature oscillators," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 1, pp. I161–I164, 2004.

[210] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-ghz cmos lc quadrature vco," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, 2002.

[211] S. Voinigescu, D. McPherson, F. Pera, S. Szilagyi, M. Tazlauanu, and H. Tran, "A comparison of silicon and iii-v technology performance and building block implementations for 10 and 40 gb/s optical networking ics," *International Journal of High Speed Electronics and Systems*, vol. 13, no. 1, pp. 27–57, 2003.

[212] T. Djurhuus, V. Krozer, J. Vidkjaer, and T. Johansen, "Nonlinear analysis of a cross-coupled quadrature harmonic oscillator," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 52, no. 11, pp. 2276–85, 2005.

[213] J. Vidkjaer, *Class Notes, 31415 RF-Comm. Circ.*, ch. VI, Oscillators. DTU, 2004.

[214] J. Van Der Tang, P. Van De Ven, D. Kasperkovitz, and A. Van Roermund, "Analysis and design of an optimally coupled 5-ghz quadrature lc oscillator," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 657–661, 2002.

[215] J. Vidkjaer, *Class Notes, 31415 RF-Comm. Circ.*, ch. II, RF-Circuits. DTU, 2004.